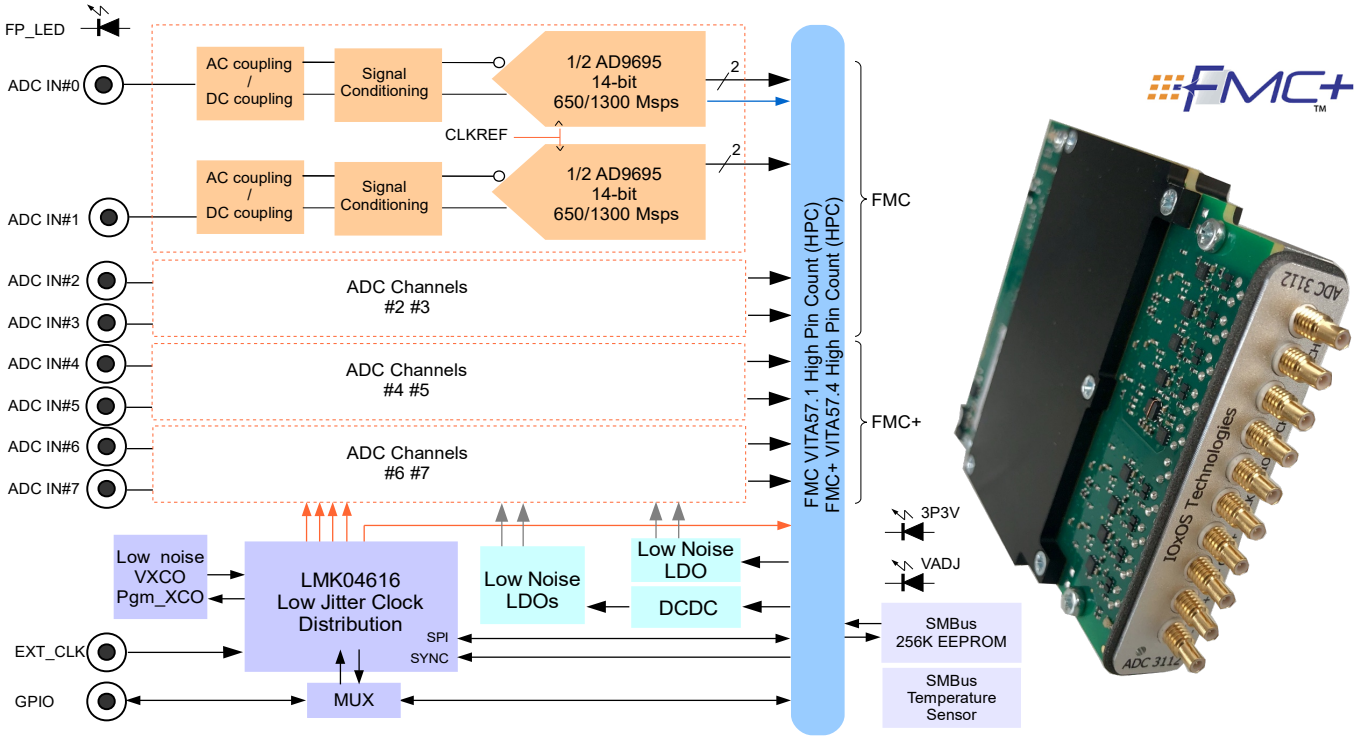
ADC_3210/3211 FMC+ Module
High Speed 14-bit ADC @ 1'300/625 Msps

ADC_3210/3211 – 8 x Channel 14-bit ADC @ 1'300/625 Msps

Building the Next Generation of Control Systems — Data Sheet



Key Features

- Eight/Four (8/4) channels
  - ✔ 14-bit @ 1'300/625 Msps with on chip DDC
- Single width FMC VITA 57.1-2008 / (FMC+)
  - ✔ HPC 400 (560) pins connector
  - ✔ 8.5/10.0 stacking option
  - ✔ Ten(10) SSMC front panel connectors
  - ✔ 4-7[W] typical power consumption
  - ✔ JESD204B signaling (2 lanes per ADC channel)
- Based on latest generation ADC technology
  - ✔ AD 9695 dual 14-bit @ 1'300/625 Msps
  - ✔ Single ended AC coupling (ADC_3210)
  - ✔ Single ended DC coupling (ADC_3211)
  - ✔ JESD204B ADC read-out interface
- Sophisticated clock tree distribution
  - ✔ TI LMK04616(dual PLL)
  - ✔ On-board ultra-low noise oscillator VCXO or Programmable XCO/VCXO
  - ✔ External SSMC Clock reference
- On board low noise power supplies generation
- Temperature sensor monitoring through SMBus
- Xilinx Ultrascale/Zync+ FPGA VHDL Design Kit
- LINUX Software Library
- Generic SCOPE AP_Specific

Overview

IOxOS Technologies introduces the ADC_3210/3211, a FMC VITA 57.1-2008 / FMC+ VITA 57.4-201 form factor featuring eight (8) ADC channels of 14-bit at 1'300/625 Msps.

The ADC_3210/3211 is the first member of IOxOS Technologies FMC+ VITA 57.4 data acquisition product line based on latest AD ADC high-speed low-power generation with digital read-out through JESD204B interface, operating from 6.25 Gbps up to 13 Gbps.

The eight(8) single-ended 50 Ohms analog inputs are supplied through SSMC high frequency connectors. AC coupling (ADC_3210) and DC coupling (ADC_3211) versions are available. Each ADC channel can optionally be connected to a wide-band digital down-converter (DDC) block, featuring decimation and low-pass / high-pass / band-pass filtering as well as digital I/Q mixing.

Clock tree is implemented with a high precision on-board low jitter low phase noise clock controller LMK04616, fully programmable by the carrier-board. The clock reference source is selectable from front panel SSMC input, FMC/FMC+ clock source or from an on-board ultra-low phase noise VCXO / programmable XCO.

The FMC/FMC+ ADC_3210/3211 incorporates precise synchronization mechanism for the dual PLL on-board clock controller LMK04616 and/or ADC devices allowing to keep in phase several units.

A user programmable GPIO SSMB can be defined as user specific TRIGGER, GATE, on-board PLL synchronization for CLOCK replication or any user specific function embedded in the carrier FPGA. A high-speed compactor with programmable level (DAC) is inserted in the GPIO input path.

The ADC_3210/3211 targets the following applications:

- Test measurement equipment
- Radar/Sonar
- Scientific / Physics experiments
- Accelerator control

EPICS

XILINX ALLIANCE PROGRAM

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Product Overview

IOxOS Technologies introduces the ADC_3210/3211, FMC/FMC+ VITA57 module featuring a high density ADC 14-bit @ 1'300/625 Msps based on latest generation Analog Devices ADC AD9695 with JESD204A read-out interface.

ADC Converter options

The ADC_3210/3211 can be equipped with following TI family pin compatible VQFN72 dual channels analog-digital converters.

ADC Device	Resolution	$Msps_{max}$	SNR(dB)	ENOB(bits)	SFDR(dB)
ADS9695-625	14-bit	625	67.2	10.6	79
ADS9695-1300	14-bit	1'300	65.6	10.5	78

At f_{IN} = 170 MHz and $Msps_{MAX}$

AC coupling front-end (ADC_3210)

The ADC_3210 50 Ohms AC coupling input is designed to be as direct to ADC as possible, in order to preserve the outstanding ADC performances. Only a Mini-Circuit TCM2-33WX+ RF transformer and a broadband matching network are used, producing a bandwidth from 10 to 800 MHz with a input VSWR < 1.5 (TBC). A low pass filter can optionally be mounted upon user request. The ADC full scale input can be changed from 0.5 to 1.9 Vpp via the SPI interface.

DC coupling front-end (ADC_3211)

The ADC_3211 implements a 50 Ohms single-ended DC coupling input stage built with the ultrahigh dynamic range TI LMH5401 differential amplifier. Gain is set by default to a nominal input range from -0.5[V] to +0.5[V].

The amplifier output is low-pass filtered at 600 MHz, limiting the global SNR reduction to about 3 dB. Amplifier THD is < -80 dBc up to 300 MHz.

JESD204B Interface

Each ADC channel read-out is supported through dual lanes JESD204B operating at 6.25 Gbps (625 Msps) or 13 Gbps (1'300 Msps).

Based on same PSW, the ADC_3210/3211 four channels variant uses an FMC VITA57.1 while the eight channels variant is developed in FMC+ VITA57.4 form factor.

Clock Distribution

The on-board clock distribution is implemented with an ultra-low phase noise / low jitter (< 100 fs) dual PLL clock driver TI LMK04616 with input clock source selected either from :

- Front panel AC coupled SSMC "CLKREF" as reference frequency for single or dual PLL mode (reference jitter cleaning via on-board VCXO)
- Front panel AC coupled SSMC "CLKREF" as direct sampling clock distribution mode or as external clock reference
- On-board ultra-low phase noise on-board 100 MHz VCXO or programmable XCO
- FMC carrier board

Four(4) output clocks (with programmable delay in steps of 25ps) are dedicated to the four(4) ADC devices, eight(8) SYSREF + GBTCLK clocks dedicated to the JESD204A interface and four(4) clocks to the FMC/FMC+ CLK0/1_M2C. The LMK04616 can also be synchronized through a SYNC input received either from the front panel GPIO SSMC or from the carrier board.

The LMK04616 is fully programmable by means of an SPI Bus driven from the carrier board FPGA.

Power Supplies

The ADC_3210/3211 on-board power supplies are built locally with low noise devices. A power tree using pairs of DC-DC and LDO regulators is derived from FMC/FMC+ 3P3V 12P0V and VADJ supplies, generating:

- Low noise 5.0 [V] for front-end amplifiers (ADC_3211)
- Low noise 3.0[V] and 1.9 [V] for ADC devices
- Low noise 3.3[V] for LMK04616 + CCHD-575/VCXO
- The DC-DC operating frequency can be synchronized by the carrier board

Other VITA57 Resources

The ADC_3210 also includes two connected SMBus devices:

- EEPROM 256K
- Temperature sensor TMP102 on the AD9695 PCB layout

TOSCA FPGA Design Kit

IOxOS Technologies provides a complete FPGA Design Kit optimized for Xilinx UltraScale/Zync FPGA family using VHDL as hardware description language, to interface the ADC_3210/3211 with the carrier's central FPGA. In addition, the design environment also includes:

- JESD204B Data Acquisition Management
- SPI Bus controller for AD9695s and LMK0461
- I2C Bus controller for LT2489 and LMK61
- GPIO, LEDs, and basic control functions

Generic SCOPE

The Generic_SCOPE is a data acquisition sub-system with functionalities similar to a oscilloscope. It is fully supported by IOxOS Technologies FMC carrier boards in VME64x (IFC_1211) and MTCA.4 (IFC_1410/1411) form factors.

Two sampling memory resources are supported:

- DDR3L storage up to 1 GBytes, @4 GBytes/s
- DPRAM storage up to 2 MBytes, @20 GBytes/s

Firmware/Software Support

IOxOS Technologies provides an FMC/(FMC+) carriers product line of VME64x (IFC_1211) and MTCA.4 (IFC_1411) supporting the ADC_3210-XX-YY-Z-LP-A0. A TOSCA FPGA design environment including FPGA firmware (VHDL sources and binary files), LINUX libraries and data acquisition design examples is also available.

This comprehensive tool allows the implementation of high-performance systems featuring the ADC_3210/3211 modules, through a fully functional application called Generic_SCOPE.

IOxOS Technologies also provides design services for the development of custom applications for Xilinx based systems.

Consult IOxOS Technologies for more detailed technical data (ENOB, SNR, SFDR Performance).

Ordering Information

Article Reference	*Product Description*
ADC_3210-XX-YY-Z-LP-A0	AC coupling version
ADC_3211-XX-YY-Z-LP-A0	DC coupling version

XX : Resolution → 14 : 14-bit
YY : Speed → 06: 625 Msps / 13 : 1300 Msps
Z : Channels numbers → 4 : Four channels / 8 : Eight channels
LP: Low pass filter: 00: filter bypass / nn: upon customer request
V : VCXO option

For other configurations please contact IOxOS Technologies

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