TOSCA II
Xilinx Virtex-6T FPGA Design Kit

Data Sheet
TOSCA_II_FDK_DS_A1

Features

- FPGA Design Kit for high-end applications development
- Hardware platform independent
- Network on Chip (NoC) solution
- VHDL source code available
- Full support provided at Hardware, Firmware and Software levels
- Drastically reduce development time, focusing on the user application

PCI Express-Centric Architecture

- Transaction Layer Packet (TLP) data packets routed through configurable full mesh switches
- Segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane)

Hardware Environment

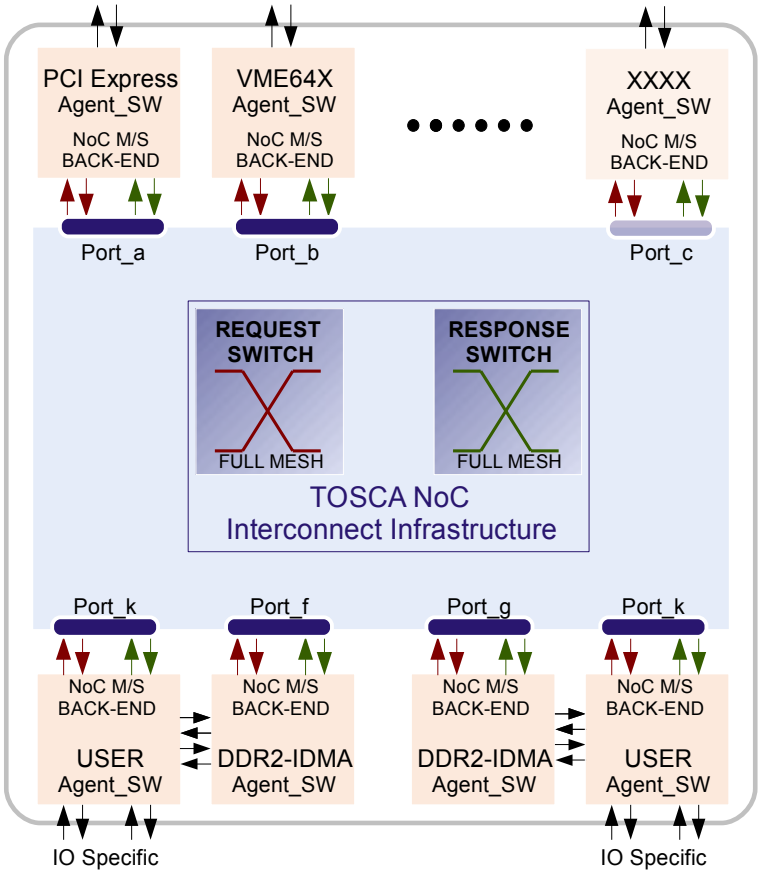
- Targets Xilinx Virtex-6T device family
- Full simulation environment and Bus Functional Models (BFM) provided
- Extensive procedures library along with tutorials and reference designs
- Implementation based on standard Xilinx design tools (XST & ISE 11.x)
- MPC_1200 and IFC_1210 Hardware Platforms available

Software Environment

- Device Drivers and User Library
- XprsMON Monitor
- FPGA bit stream remote update
- Built In Test capability

IOxOS IP Core Library

- TOSCA NoC Full Mesh Central Switch (x8)
- PCI Express GEN2 EP Wrapper
- DDR3 Multi-port Memory Controller
- Intelligent Chained DMA Controller
- I2C, SPI and SRAM Controllers
- VME64x Master/Slave
- Fast ADC Interface
- MPF IO Module basic Interface
- Spartan-6 data concentrator



Overview

Field Programmable Gate Arrays (FPGAs) are gaining acceptance as a powerful platform for many applications in today's industry due to their speed, embedded features and flexibility. The continuous increase in terms of complexity of these applications combined with shortening time to market requirements have lead to structural optimization in FPGA design and the use of intellectual property (IP) cores. The most challenging issue FPGA designers face is the integration of their application with all the IP cores necessary to implement a fully functional FPGA.

To overcome this challenge, IOxOS Technologies SA releases the TOSCA II FPGA Design Kit solution, a comprehensive FPGA design environment which provides full visibility and facilitates the integration of the user application within a high-performance PCI Express switch-centric architecture. This approach makes possible the implementation of a complete Network on Chip (NoC) solution which includes a PCI Express endpoint, DDR2 memory controllers, intelligent DMA engines, Multi Root I/O Virtualization and embedded user areas tightly coupled with these built-in resources.

The TOSCA II FPGA Design Kit provides RTL and behavioral VHDL source code together with reference designs, access to the IOxOS IP core library, a set of test-benches and Bus Functional Models.

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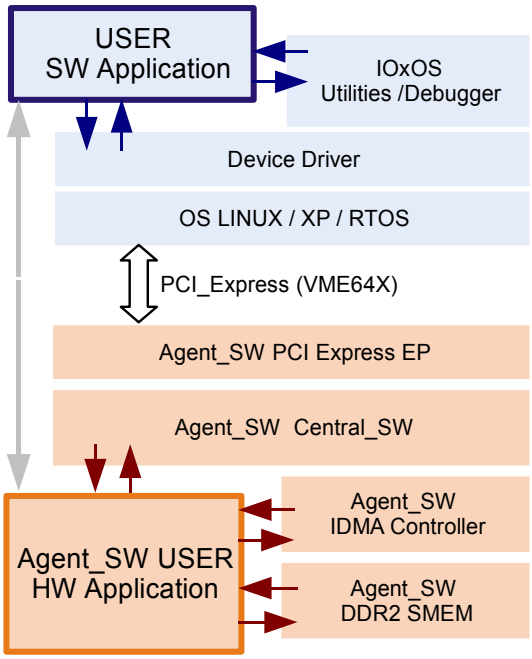
Introduction

Conventional design kits offer a set of IP cores along with implementation examples. IOxOS Technologies SA goes one step further releasing the TOSCA II FPGA Design Kit, a comprehensive system oriented design environment that covers all the path, from the software application to the FPGA user code.

Every Software element (OS device drivers, utilities and debugging tools) is fully integrated within the Hardware environment (bus interfaces, I/O & Configuration space, embedded DDR3 controllers, intelligent DMA engines and interrupt managers inter alia).



The allocated FPGA user area can be implemented with VHDL or the following high-level tools methodologies in order to fulfill the most demanding applications such as signal processing or high performance computing. Soft IP microprocessors, such as Xilinx MicroBlaze, can be easily integrated in the FPGA user area with full remote control over the PCI Express infrastructure.

FPGA Technology Trends

Today's high-performance 40nm FPGA devices such as Xilinx Virtex-6T family, provide a very high density of logic resources. Even the smaller part (XC6LX130T) can host a complete NoC system.

All these facts along with FPGA inherent parallelization capabilities make these devices a very powerful and attractive platform to implement DSP or mathematical algorithms.

To make the most of FPGA current and future features, TOSCA II FPGA Design Kit is ready for the next FPGA generation, offering the TOSCA architecture, a fully scalable NoC solution with configurable IP cores and based on well established technologies with long term life cycles, such as PCI Express and Ethernet as well on legacy systems as VME64X

NoC Architecture

The Network on Chip (NoC) solution is an alternative to the traditional bus-based architectures widely used in System on Chip (SoC) implementations. This alternative has proven to be plenty of benefits:

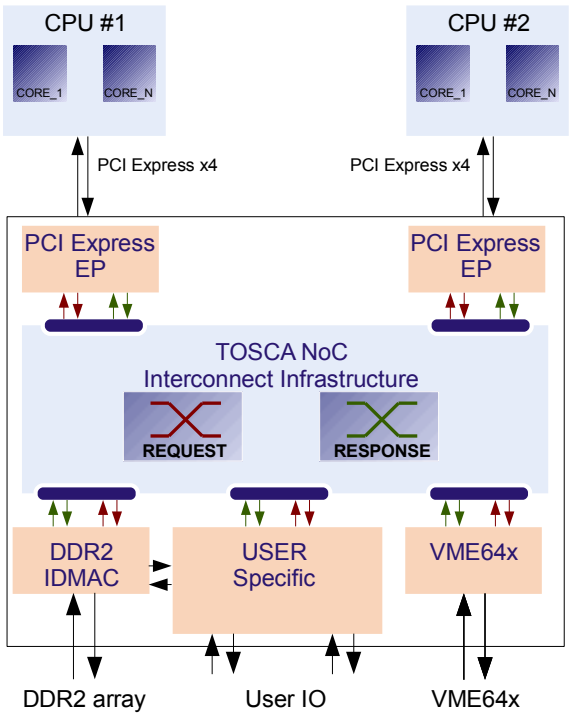
- Scalability and growing capabilities
- Increased point to point bandwidth (> GBytes/s)
- Controlled latency with best in class Quality of Service (QoS)
- Easier verification due to modular approach

The TOSCA II architecture is based on a NoC approach which uses PCI Express as legacy network, routing PCI Express Transaction Layer Packet (TLP) data through configurable full mesh switches. Each TLP is composed of a TLP Header, a data payload and an optional TLP digest field for ECRC purposes.

This PCI Express centric implementation provides a de-facto standard packet structure in order to support Single or Multi Root I/O Virtualization (SR_IOV and MR_IOV capabilities referenced in the new PCI Express specification released by the PCISIG), which is a key element for the upcoming generation of multi-core microprocessors and embedded systems.

Reference Design Example

The following diagram provides an example of a TOSCA II architecture based application which can be implemented using TOSCA II FPGA Design Kit available resources. A dual multi-core CPU system on a VME64x Single Board Computer (SBC) with a Virtex-6T FPGA on board. The FPGA interfaces both multi-core CPUs with the VME64x backplane, providing user specific I/O control and local DDR3 shared memory access with DMA capability.



TOSCA II Architecture Overview

The TOSCA II architecture is based on a PCI Express switch centric structure which implements a memory mapped model with segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane)

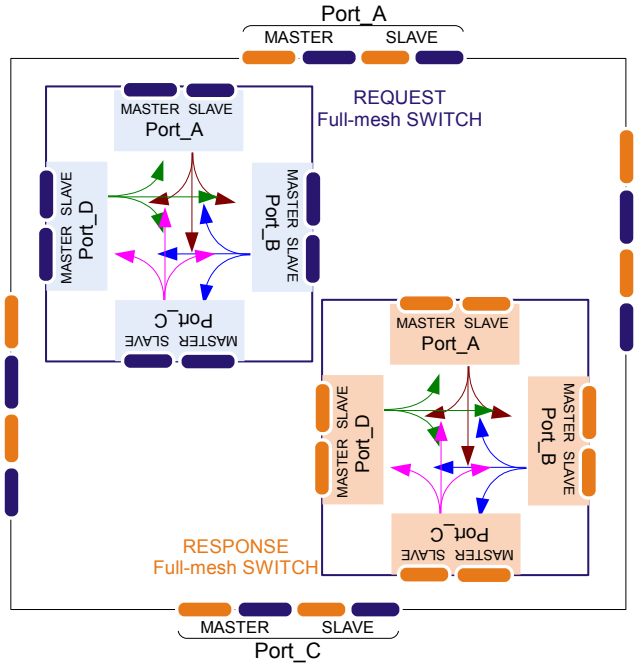
The CONTROL Plane implements the I/O Space Read/Write transactions, initialization tasks and interrupt handling. The IO_Bus, a 32-bit Master/Slave IOxOS proprietary bus, supports these facilities across the different modules (referenced as Agent_SW) connected to the central switch. The DATA plane implements the Memory Space Read/Write transactions with optimal data rate performance across a switched NoC infrastructure.

TOSCA II Central Switch

The TOSCA II architecture main core is the TOSCA Central Switch (referenced as Central_SW), a N-port dual full mesh non blocking switch. Both Request and Response switches integrate INgress and OUTgress TLP buffer queues (FIFO) providing an optimal data transfer bandwidth.

Thanks to its full mesh interconnection, each TOSCA Central_SW port can provide the following four independent back-end interfaces, able to run simultaneously at full speed (i.e 64-bit @ 200MHz ~ 1.6 GBytes/s):

- Master Write_Request – Read_Request
- Master Read_Response
- Slave Write_Request – Read_Request
- Slave Read_Response



The TOSCA II Central_SW is fully configurable and can be customized up to 8 ports. A 64-bit 4-port TOSCA Central_SW (default configuration) running at 250 MHz provides an aggregate bandwidth of 2 x 4 x 2.0 GBytes/s = ~ 16.0 Gbytes/s.

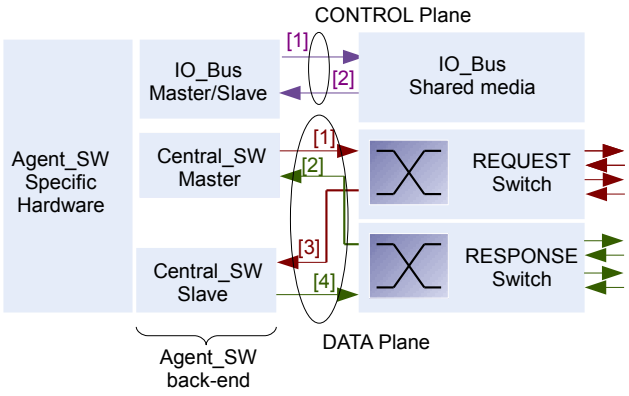
The routed data packets are directly based on PCI Express TLP format. Additional 16-bit information is added to the TLP Header providing the switch with self-routing information (Source & Destination Port Number) and flushing management. Based on the Source information, TLP are sorted in separate queues, preventing the Slave to be blocked by a single Master.

The INgress and OUTgress buffer queues, implemented with true DPRAM on every back-end interface, allow the TOSCA Central_SW back-end interfaces to run in their own time domain.

Agent_SW

The following TOSCA Agent_SW IP cores are supplied :

- PCI Express GEN2 EP/RC Wrapper
- DDR3 Multi-port & IDMA Controllers
- VME64x Master/Slave
- USER Block



The Agent_SW CONTROL plane back-end is handled by the following two (2) IO_Bus interfaces:

1. Master IO_Bus Read/Write, used by local intelligent resources such as embedded processors (i.e MicroBlaze)
2. Slave IO_Bus Read/Write used to map I/O Space resources

The Agent_SW DATA plane back-end is handled by the following four (4) interfaces, all of them implemented through a 64-bit back-end running at 100-250 MHz:

1. Master Tx Read_Request and Write_Request
2. Master Rx Read_Response
3. Slave Rx Read_Request and Write_Request
4. Slave Tx Read_Response

Each interface can be active concurrently, providing a global data-rate of 6.4 GBytes/s per Agent_SW, and interfaced to the TOSCA II Central_SW with its own time domain, simplifying the IP integration.

Thanks to its memory mapped model, two Agent_SW connected through the TOSCA Central_SW can deploy a transparent Bus Bridge function as long as an address remapping capability is provided. As an example, when both PCI Express EP Wrapper and VME64x Agent_SW are instantiated, transparent bridging between PCI Express and VME64x is supported.

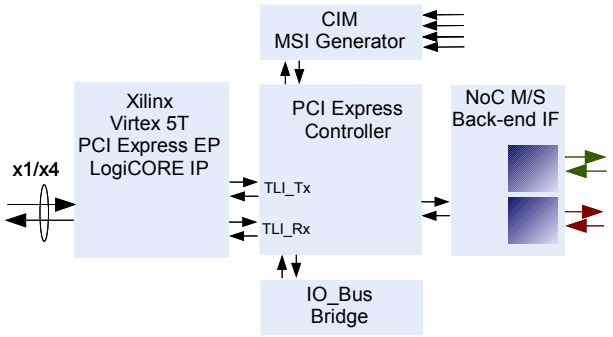
Both PCI Express EP Wrappers and VME64x Agent_SW integrate programmable INgress MMU supporting address remapping and physical switch port allocation based on

source address information.

A fully functional PCI Express EP to VME64x Transparent Bridge function is implemented on the MPC_1200 and IFC_1210 Hardware Platforms using the TOSCA II FPGA Design Kit.

PCI Express EP Wrapper Agent_SW

The PCI Express GEN2 EP Wrapper Agent_SW, built on top of the Virtex-6T embedded PCI Express EP LogiCORE IP, is the default Host Interface for the TOSCA II FPGA Design Kit. All software utilities, running under PC or Workstation deploy this interface.



The PCI Express Controller module interfaces the PCI Express EP LogiCORE IP Transaction Layer Interface (TLI) protocol and the on-chip TOSCA II infrastructure. The TLP packets decoded in I/O Space are sent to an IO_Bus Master controller, providing a direct mapped access to all Agent_SW I/O Space area. The TLP packets decoded in Memory Space are reformatted to TOSCA II NoC format and sent across the NoC infrastructure. Address remapping and NoC routing are supported through a programmable INgress MMU.

The Central Interrupt Manager (CIM) module handles the on chip system interrupts and dispatch them through the PCI Express Message Signaled Interrupt (MSI) interface.

The TOSCA II architecture can support up to two (2) PCI Express EP Wrapper Agent_SW in Virtex-6T devices.

VME64x Agent_SW

The VME64x Agent_SW implements a fully functional VME64x Master/Slave Interface with Slot-1 function capability. It handles all data transfer types defined by the VME64x VITA standard (SBT, BLT32, MBLT64, 2eVME & 2eSST) and integrates configurable byte swapper capability (hardware)

→ *Programmable slave window*

→ *Bridge capability*

→ *Big-Little Endian conversion*

→ *External transceivers*

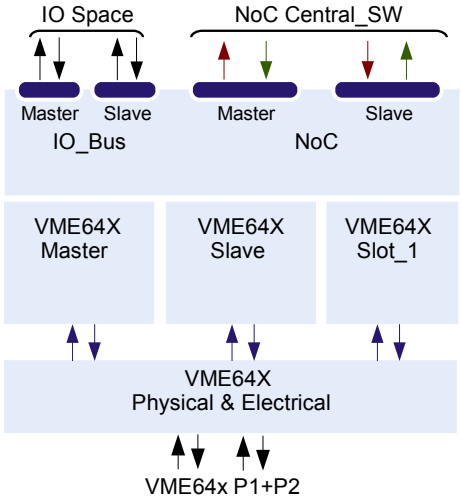
→ *Central arbiter + BTO/2eBTO*

→ *Interrupt handler*

→ *Cycle optimizer*

The VME64x Master is a memory mapped Interface acting as transparent bridge, directly accessible from the following blocks Agent_SW:

- PCI Express EP Wrapper
- DDR2 Multi-port & IDMA Controllers
- USER Block



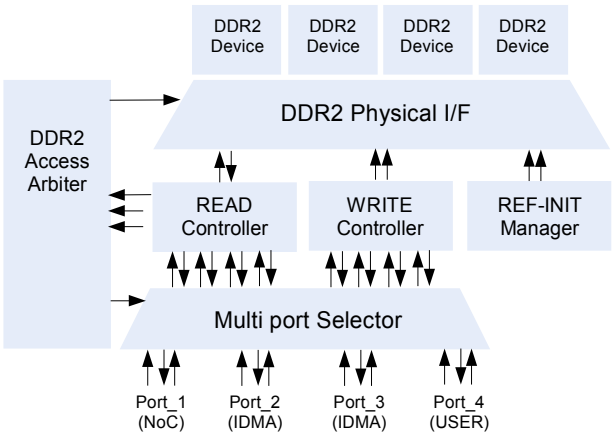
The VME64x Slave module allows to map internal resources over the VME A32 addressing space. A programmable INgress MMU, divided in pages of 1 MBytes, allows to remap the VME addressing space to the internal TOSCA address mapping.

The VME64x Agent_SW also integrates some specific functions:

- VME Error handling support
- Programmable Interrupt Generator
- Global 48-bit Timer with external synchronization through IRIG-B or direct VME signaling

DDR3 Multi-port Memory Agent_SW

The DDR3 Multi-port Memory Agent_SW implements a complete DDR3 controller with segregated Read and Write data accesses. The multi-port arbitration algorithms as well as dynamic port enabling are selectable, providing best in class QoS.



The DDR3 memory array is accessible through the Port_1 (NoC) for every Agent_SW connected to the TOSCA

Central_SW .

The DDR3 Multi-port Memory Agent_SW supports up to 4 ports

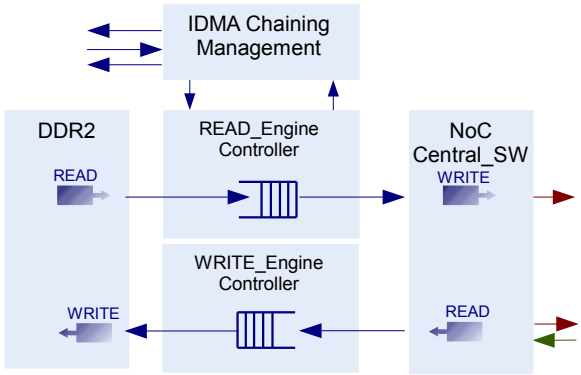
- Port_1 : TOSCA Central_SW Slave port (NoC)
- Port_2 : IDMA Controller Descriptor Fetch & Update
- Port_3 : IDMA Controller data
- Port_4 : Private USER Block Agent_SW

The DDR3 Memory Controller is tightly coupled through Port_2 and Port_3 to the embedded IDMA Controller Agent_SW to optimize DMA accesses to the DDR2 array.

IDMA Controller Agent_SW

The IDMA Controller Agent_SW implements a multi-channel chained DMA controller. Data transfer is handled autonomously between the DDR3 memory array and the NoC infrastructure. The IDMA Controller Agent_SW uses two independent engines (Read_Engine and Write_Engine).

The Read_Engine reads data from the DDR3 array memory and send them to the NoC infrastructure (to any of the Agent_SW) or to its Direct_OUT port. The Write_Engine reads data from the NoC infrastructure (from any of the Agent_SW) or from its Direct_OUT port and send them to the DDR3 array memory.

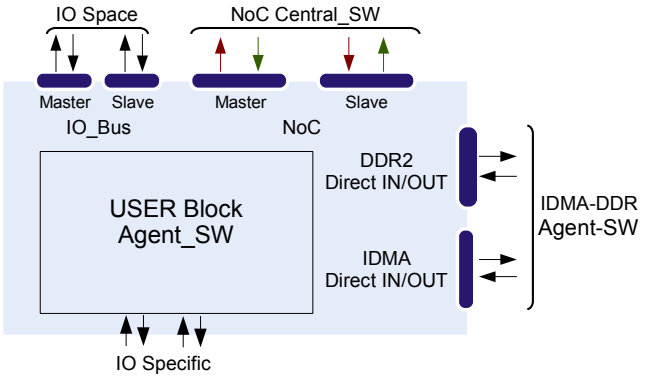


The Direct_OUT and Direct_IN ports are both connected to the USER Block Agent_SW to provide the user with a fast access to this resource.

Each DMA channel has chaining capability (up to 16 MBytes per chain-descriptor) and is associated to an “End of Transfer” Interrupt, coupled to status and time-stamp information. The DMA engines are controlled by a set of registers mapped into the I/O space, the chain descriptors are located in the DDR3 memory. The DMA engines implement an inter-engine triggering capability which allows to start a 2nd engine on condition occurred on a 1st engine. The DMA Write_Engines are able to issue multiple outstanding Read_Request to support optimal PCI Express read performance.

USER Block Agent_SW

The FPGA area and logic resources allocated to the user application are embedded in the USER Block Agent_SW. Multiple USER Block Agent_SW can be instantiated in a TOSCA II architecture. As any other Agent_SW, the USER Block Agent_SW has access to the predefined interfaces with the NoC infrastructure but also integrates a direct connection with the DDR3 and IDMA Controller Agent_SW.

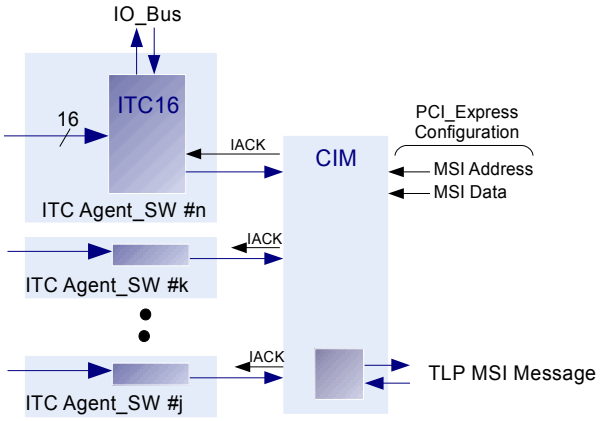


Each USER Block Agent_SW is provided with the following ports:

- IO_Bus Slave port to interface the USER Block Agent_SW with the I/O Space infrastructure (1KByte per Agent_SW).
- IO_Bus Master port to support local intelligent modules such as embedded processors (i.e. MicroBlaze).
- NoC Slave port to map the USER Block Agent_SW into the TOSCA MEMORY Space. It provides support for Write_Request, Read_Request and Read_Response.
- NoC Master port to provide the USER Block Agent_SW with full access to the NOC infrastructure.
- DDR3 direct path to provide a simple Read/Write interface to the DDR2 Multi-port Memory Agent_SW. It allows the USER Block Agent_SW to access the DDR2 array without implementing the complete NoC Master controller.

Interrupt Support

Each Agent_SW integrates a 16-input Interrupt Controller (ITC16). When an Interrupt is locally detected, the event is sent to the Central Interrupt Manager (CIM) which manages all ITC16 instantiated. The CIM controller is usually integrated in the PCI Express EP Wrapper Agent_SW and generates PCI Express MSI Messages. The MSI parameters (MSI Address / MSI Data) are initialized by the Host Controller.



Other IP Cores Provided

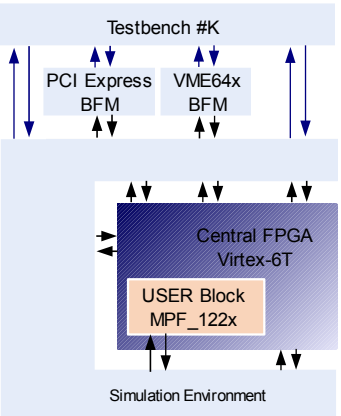
To make the system integration faster and easier, the TOSCA II FPGA Design Kit includes a VHDL IP core library with the following complementary functions:

- I2C Master Controller
- Virtex-6T System Monitor interfaces to on-chip IO_Bus
- Virtex-6T PCI Express LogiCORE interfaces to on-chip IO_Bus
- External FPGA configuration from SPI Serial Flash
- Power On Finite State Machine (PON_FSM) micro-programmed controller to manage system initialization from external SPI Flash EPROM
- Virtex-6T System Monitor controller

FPGA Simulation Environment

The TOSCA FPGA Design Kit is delivered with full VHDL source code together with a set of test-benches and Bus Functional Models (BFM) to set up a complete VHDL simulation environment for functional verification purposes. This simulation environment is supported by the main HDL simulation tool vendors (Mentor Graphics ModelSim and Aldec Riviera).

- PCI Express LogiCORE TLI Target/Initiator
- VME64x Master/Slave with direct support of SBT, BLT32, MBLT64, 2eVME & 2eSST



FPGA Physical Implementation

The FPGA physical implementation is based on the following standard Xilinx design tools (no 3rd party VHDL synthesis tool required):

- Synthesis: Xilinx XST (included in Xilinx ISE 11.x)
- Place & Route: Xilinx ISE 11.x
- PROM file generation: Xilinx iMPACT

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A complete set of tutorials and reference designs are also supplied to guide the designer through all the implementation and verification flow.

Software and Services

The TOSCA FPGA Design Kit is supported with the following software items:

- LINUX device drivers (PCI Express & VME64x)
- User library with examples
- XprsMON and FPGA Built utilities

XprsMON is a Linux application linked with the TOSCA user library which allows the user to interactively perform a set of commands to operate the TOSCA infrastructure :

- Patch, Examine, Deposit & Display operations on Memory and I/O Space references
- Patch, Examine, Deposit & Display operations on VME64x references
- Exercise Interrupts, Global_Time and DMA capabilities
- Built In Test (BIST) and Configuration support
- Flash Memory programming (FPGA bit stream download)

Licensing

The TOSCA II FPGA Design Kit is delivered with full RTL and behavioral VHDL source code. This source code is provided under NDA and can not be supplied to 3rd partis. The TOSCA FPGA Design Kit basic package includes a 5 days training and 100 run-time (RT) licenses. Additional RT licenses are available upon request.

Learn more: info@ioxos.ch

Ordering Information

Article Reference	*Product Description*
TOSCA1102-BAS	TOSCA II FPGA Design Kit Basic Package • Complete VHDL Source files • 5 days training • 100 FPGA RT licenses
TOSCA1102-RT1	200 FPGA RT licenses
TOSCA1102-RT2	500 FPGA RT licenses
TOSCA1102RT3	1K FPGA RT licenses