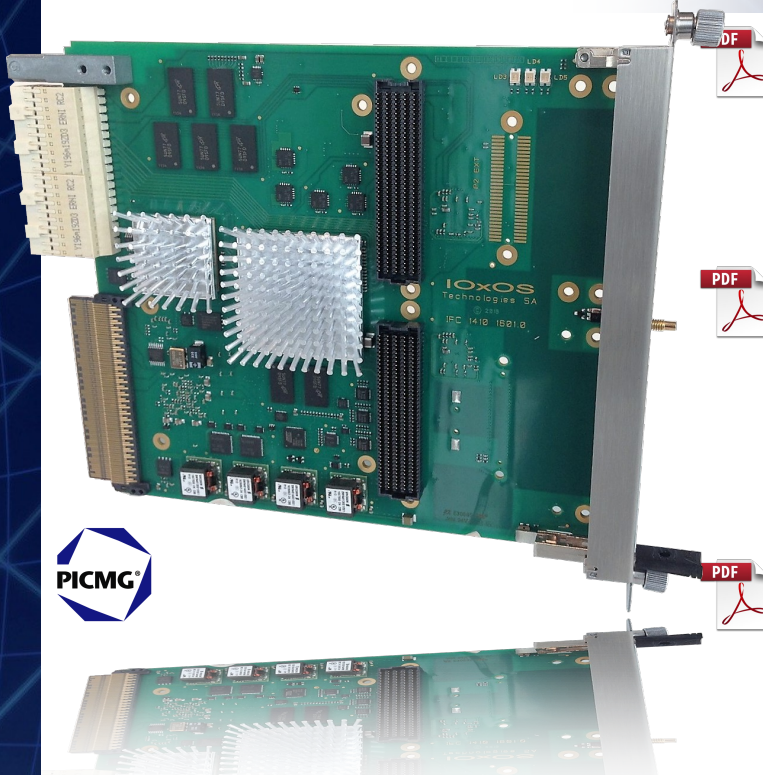


MTCA.4 Complete Ecosystem



MTCA.4 Product Line of AMCs and μ RTMs



IFC_1410 Intelligent FMC Carrier AMC

NXP QorIQ T2081 @ 1.8 GHz with Altivec
Xilinx Kintex UltraScale FPGA (KU040 / KU060)
Powered by TOSCA III FPGA Design Kit
Dual HPC VITA 57.1 FMC slots
DESY D1.4-compliant RTM interface

IFC_1420 High-Performance Digitizer AMC

NXP QorIQ T2081 @ 1.8 GHz with Altivec
Xilinx Kintex UltraScale FPGA (KU040 / KU060)
Powered by TOSCA III FPGA Design Kit
10 channels ADC 16-bit @ 250 Msps (from RTM)
5 channels DAC 16-bit (to RTM)
Single HPC VITA 57.1 FMC slot
DESY A1-compliant RTM for analog signals

RSP_1461 Com Extender μ RTM

One SFP Gigabit Ethernet
Six SFP+ (10 Gigabit Ethernet & user-defined SerDes)
Two SMA connectors for clock I/O
DESY D1.4-compliant RTM interface

Comprehensive Family of FMC Modules

FMC VITA 57.1 HPC including firmware integration (VHDL) and EPICS support

ADC_3110/3111

8 channels ADC 16-bit @ 250 Msps
AC or DC coupling inputs
Clock & user-defined inputs



DAC_3113

Dual channel ADC 16-bit @ 250 Msps
Dual channel DAC 16-bit @ 250 Msps
DC coupling
Clock & user-defined inputs



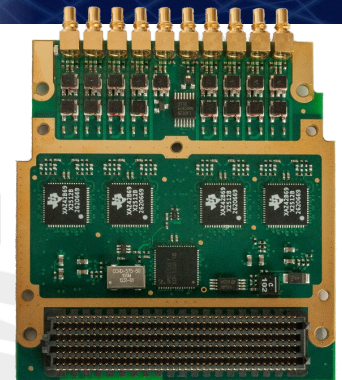
ADC_3112

4 channels ADC 12-bit @ 1 Gbps or
2 channels ADC 12-bit @ 2 Gbps
DC coupling inputs
Clock & user-defined inputs



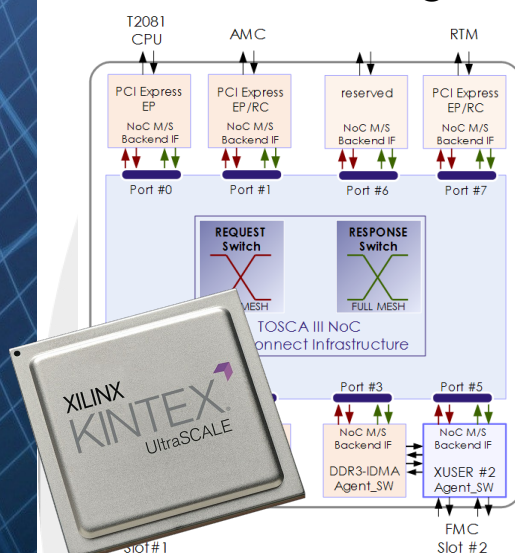
ADC_3117

20 channels ADC 16-bit @ 5 Msps
2 channels DAC 16-bit @ 1 Msps
Single ended or differential input
Clock & user-defined inputs



VITA
Open Standards, Open Markets

TOSCA FPGA Design Kit & EPICS Integration



FPGA Design Kit optimized for Xilinx Kintex UltraScale devices

Network on Chip (NoC) approach

Up to three PCI Express GEN3 blocks (End Point/Root Complex)

VHDL source code fully available

Straight-forward integration of FMC within MTCA.4 AMC carriers

Significant reduction of development time by:

- ✓ Focusing on user application
- ✓ Granting access to IOxOS Technologies IP Core library
- ✓ Providing User Area dedicated simulation environment
- ✓ Including reference designs

Total integration within EPICS ecosystem

