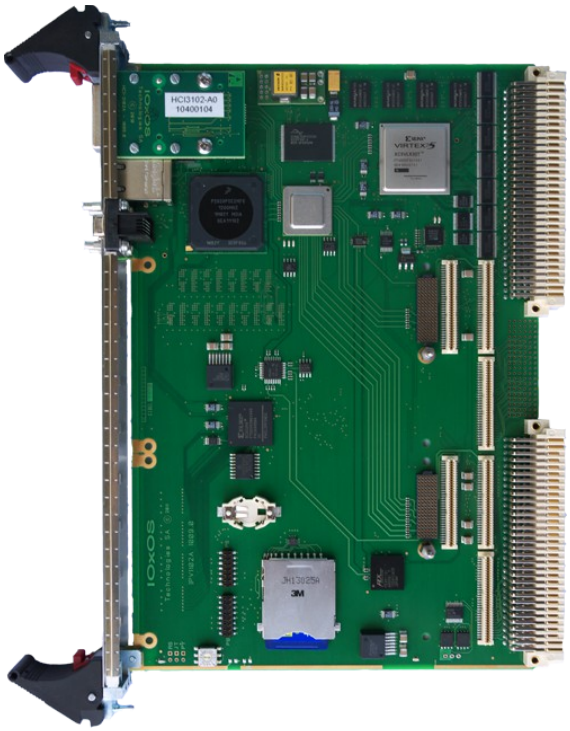
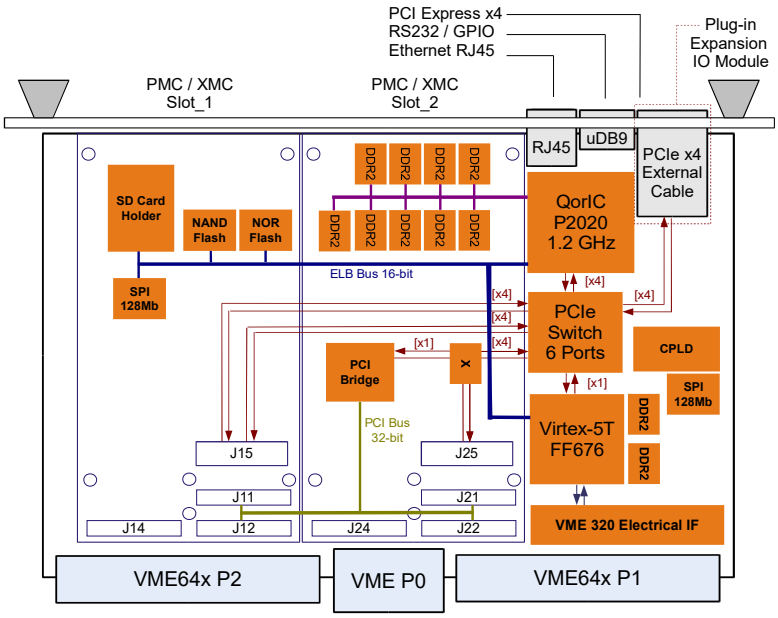
IPV_1102 - Intelligent PCI Express / VME64x P2020 VME64x Single Board Computer

Data Sheet IPV_1102





Features

- 6U VME64x Single Board Computer
- Commercial temperature grade
- Freescale PowerPC P2020 computing core
  - QorIQ P2020 1.2 GHz
  - Up to 4 GByte DDR2 System Memory
  - NAND Flash, NOR Flash
  - SD Card Holder
  - 10/100/1000 BaseT Ethernet
  - Dual RS232
- Front panel External Cabling PCI Express x4 connection (configurable:Copper/Optical)
- Dual PMC / XMC Mezzanine socket
- P2020 PCI Express operation EP or RC
- VME64x Master/Slave with 2eSST support
- Low latency VME64x access (Direct bridging PCI Express - VME64x)
- Built around Xilinx Virtex-5T FPGA
- FPGA user area for additional IO applications and/or hardware computing acceleration
- Powered by TOSCA I FPGA Design Kit
  - Network on Chip (NoC) architecture
  - Shared Memory DDR2
  - VHDL source code available

Overview

IOxOS Technologies introduces the IPV_1102, a 6U VME64x highly configurable Single Board Computer with embedded FPGA capability. The IPV_1102 is built around a high performance switched PCI Express architecture.

The IPV_1102 provides in its front panel a PCI Express extension based on PCI-SIG standard “PCI Express External Cable Specification”. This high performance extension, which can be used to connect the IPV_1102 to a workstation with a memory mapped model, is implemented as a plug-in expansion IO module to support different physical media (copper/optical).

The IPV_1102 integrates the latest generation of Freescale PowerPC QorIQ processors. The P2020 provides dual-core capability running at 1.2 GHz with low power operation (< 7[W]). It is supported with large System Memory (up to 4 GBytes), non volatile memory NOR, NAND, SD and multiple IO capabilities.

The on-board Xilinx Virtex-5T FPGA implements a high performance PCI Express centric Network on Chip (NoC) switched interconnection. This NoC architecture provides a non-blocking, controlled low-latency and high-throughput bandwidth interface between the data producer and consumer.

The VME64x interface, which is also implemented in the FPGA, is implemented with a direct transparent low latency PCI-Express / VME64x bridge. It supports all Master/Slave VME64x modes of operation with Slot_1 System Controller.

The IPV_1102 is powered by TOSCA I, a comprehensive FPGA Design Kit developed by IOxOS Technologies, which is available for the implementation and integration of custom applications within the IPV_1102 on-board Virtex-5T FPGA.

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Introduction

The IPV_1102 is a 6U VME64x Single Board Computer with a PCI Express External Cable interface in its front panel. This versatile extension (PCI-SIG standard) allows building high performance systems optimized for RT embedded applications.

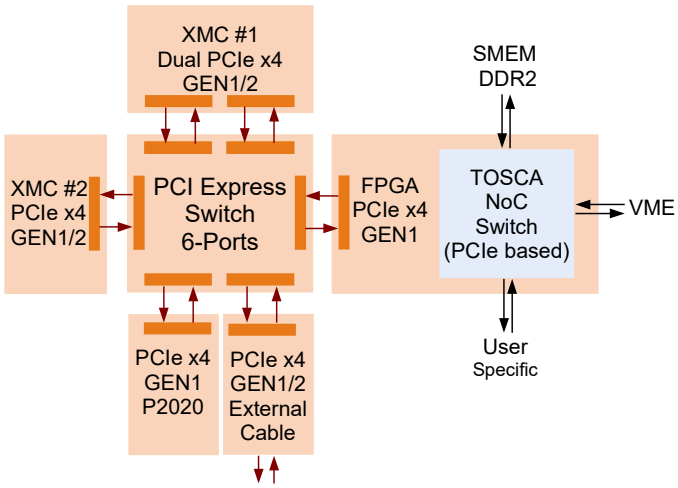
The IPV_1102 can be basically used in the following three modes of operation:

- Legacy Single Board Computer
- Standard PC Interconnect with P2020 operating in EP (Slave) mode.
- PC Interconnect with P2020 in RC and connected to external PC through a Non-Transparent (NTB) port

As a Single Board Computer, the IPV_1102 has a complete IO capability (Ethernet, RS232, SD card), extensive memory resources and optimized real-time support such as VME64x bridge, independent Shared Memory, and user specific blocks all implemented inside its high performance Virtex-5T FPGA.

PCI Express Centric Architecture

The IPV_1102 is built around the latest generation of PCI Express GEN1/GEN2 non-blocking switches, providing six (6) PCI Express x4 GEN1/GEN2 ports.



The six (6) PCI Express x4 ports are mapped as follows:

Port_0 Front panel PCI Express External Cable Interface

Port_1 P2020 Central PowerPC microprocessor

Port_5 Virtex-5T FPGA (VME64x, Shared DDR2, User area)

Port_6 XMC #2 VITA 42.3 or PCI Express-PCI Bridge for PMC support

Port_8 XMC #1 VITA 42.3

Port_9 XMC #1 VITA 42.3

The Upstream port (connected to the Root Complex) and the PCI Express clocking schema (local CFC or external SCC/CFC) are statically configurable.

Port_0 or Port_1 can also be configured in Non-Transparent mode (NTB).

The PCI Express topology is naturally extended inside the FPGA fabric by means of TOSCA I's native Network on Chip (NoC) non-blocking switch. This provides an unified PCI Express centric architecture.

The front panel PCI Express External Cabling port can be statically configured to operate in UP-stream, DOWN-stream or Non- Transparent (NTB) modes.

All six ports can operate independently in GEN1 (2.5 Gbit/s) or GEN2 (5.0 Gbit/s).

PCI Express External Cable Interface

The IPV_1102 provides a PCI Express x4 External Cable extension in its front panel (PCI-SIG Specification 1.0). This external connection allows to extends the local PCI Express infrastructure over several meters by keeping a transparent memory mapped model.

The IPV_1102 can be equipped with several expansion IO modules to support different physical media such as:

- PCI Express x4 copper up to 7 meters in GEN1
- PCI Express x1 copper up to 7 meters
- PCI Express x4 optical up to 100 meters

This external PCI Express connection allows to build real-time links combining very low latency (<1 [us]) with high sustained throughput (> 800 MBytes/s) .

The IPV_1102 can be tightly coupled with high performance multi-core workstations or servers, delivering an unprecedented performance. In this case the PCI Express External Cable connection can be configured as UP_stream port or DOWN_stream port with Non-Transparent (NTB) mode.

Additionally, the two (2) XMC slots can be equipped with the XMC_3105 module, a Dual PCI Express External Cable adapter for additional External PCI Express capability.

P2020 Computing Core Resources

The PowerPC P2020 microprocessor is supported by the following memory resources. All non-volatile resources can be selected as Bootable.

- 1, 2 or 4 GBytes DDR2-600 System Memory
- 256 MBytes NAND Flash Memory with ECC
- 16 MBytes NOR Flash Memory
- 128 Mbit SPI Serial Flash Memory

The P2020 PCI Express port can be configured as Root Complex (RC, which manages the local PCI Express enumeration) or as End Point (EP).

The P2020 enhanced Local Bus (eLBC) is also directly connected to the on-board Virtex-5T FPGA, providing a simple and direct pathway to the user area.

The microprocessor is powered by a dedicated, high efficiency DC-DC optimized for low noise environment.

P2020 IO Resources

The P2020 provides the following IO on the front panel:

- One (1) RJ45, Ethernet 10/100/1000 Base-T
- One (1) µDB9, RS232
- One (1) µDB9, Four (4) programmable GPIO (RS485)
- JTAG COP debugging socket (option)

Additionally a 2nd Ethernet 10/100/1000 Base-T and a 2nd RS232 are available through the VME P0 connector.

VME64x Legacy Interface

The Central Virtex-5T FPGA embeds a proprietary IP Core providing a complete Master/Slave VME64x interface. Thanks to the direct PCI Express to VME64x bridge (with no intermediate PCI Bus), it provides a very low latency access. The electrical interfacing is based on VME320 ETL technology, supporting both full speed 2eSST and 2eVME protocols.

The VME Slave interface implements the legacy VME/VME64 addressing configuration with static switches and/or VME64x CR/CSR. The VME Slave handles all addressing modes including 2eVME and 2eSST.

The VME Master interface, driven by the internal FPGA infrastructure supports also all VME addressing modes, including 2eVME and 2eSST as well.

In addition, the VME Master integrates a complete VME Slot_1 function, Interrupt Generator/Handler and a global time synchronization distribution over the back-plane.

VME64x P2 User IO

The VME P2 user IO (rows A & C / 64 signals 32+32) are directly wired to the PMC mezzanine user IO:

- PMC Jn14 → 64 IO
- PMC Jn24 → 32 IO (static option)

VME64x P0 User IO

The VME P0 provides the following additional IO resources:

- 2nd Ethernet 10/100/1000 Base-T (without magnetics)
- 2nd RS232 (auxiliary console)
- 15 GPIO (LVTTL), wired to the Virtex-5T FPGA
- 64 User IOs from PMC Slot 2 (Jn24)

PMC / XMC Mezzanine

The IPV_1102 provides two (2) XMC/PMC Mezzanine slots for custom expansions.

The two PMC slots are controlled with legacy 32-bit PCI (33/66 MHz) bridged from the PCI Express infrastructure. The PMC User IOs (Jn14 / Jn24) are directly wired to the VME64x P2 IO extension. Two connection modes are possible.

Both XMC VITA 42.3 slots are controlled with independent PCI Express x4 interfaces, able to operate in GEN1 or GEN2. The XMC Slot 1 has two PCI Express x4 interfaces.

Both XMC slots can also be equipped with the XMC_3105 module, a Dual PCI Express External Cable adapter which allows to extend the local PCI Express infrastructure across multiple VME boards.

Global Time

A global timer, composed of one low resolution 32-bit 1[ms] + one high resolution 16-bit 10-1000[ns] is embedded in the TOSCA I infrastructure. This global timer can be kept on-time through a dedicated external synchronization mechanism:

- VME SYSFAIL# or IRQ[7:6] synchronization
- Front panel GPIO RS485 or VME P2/P0 User IO

Virtex-5T Central FPGA Support

The Xilinx Virtex-5T Central FPGA architecture is organized in a hierarchy level composed of two main blocks:

- The IPV_1102 IP Core integrating the basic carrier board infrastructure: NoC Switch, PCI Express EP, VME64x Master/Slave, DDR2 shared memory controller with IDMA and the Interrupt controller
- One User block, fully configurable by the end user for custom applications

The IPV_1102 IP Core is released in binary format (NGC), along with generic User Block examples and all needed files for the implementation of a fully functional FPGA for the IPV_1102.

The IPV_1102 supports the following Virtex-5T devices: LX30T (default), LX50T and SX50T.

Local FPGA Resources

The IPV_1102 integrates DC-DC power supplies for the on-board FPGA and for the P2020 processor. These DC-DC are dimensioned to support the whole Virtex-5T device family.

One 128 Mbit SPI Flash EPROM device is used to store the FPGA configuration bit-stream. A section of this non-volatile memory is allocated to the user application.

Four DDR2 Memory devices are wired to the Virtex-5T Central FPGA. The DDR2 IP core memory controller which provides the complete control of the DDR2 devices is part of the TOSCA I FPGA Design Kit (1 Bank @ 1.6 GBytes/s with 2 or 4 DMA channels).

The DDR2 Controller integrates an optimized multi-channel chained DMA controller able to move autonomously data from/to the DDR2 to/from the VME, PCI Express and User area.

Other functions such as the I2C and SPI interfaces, GPIO management, Power-ON FSM controller, and power supply monitoring, are integrated within the Virtex-5T Central FPGA firmware developed with the TOSCA I FPGA Design Kit.

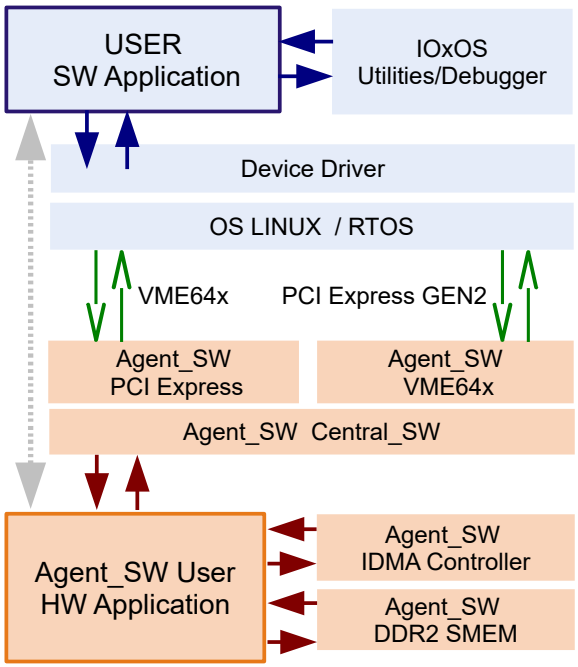
TOSCA I FPGA Design Kit

Conventional design kits offer a set of IP Cores along with implementation examples. IOxOS Technologies goes one step further releasing the TOSCA I FPGA Design Kit, a comprehensive system design environment that covers all the path, from the SW application to the FPGA user code.

The TOSCA I FPGA Design Kit can be delivered with full VHDL source code together with a set of test-benches and Bus Functional Models (BFM) to set up a complete VHDL simulation environment for functional verification purposes. This simulation environment is supported by the main HDL simulation tool vendors.

The TOSCA I architecture is based on a PCI Express switch centric structure implementing a memory mapped model with segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane).

The TOSCA I FPGA Design Kit enhances the versatility of the IPV_1102 solution, providing the user with a powerful tool for the implementation and integration of custom applications within the IPV_1102 on-board Virtex-5T FPGA.



Software Support

The TOSCA I FPGA Design Kit is supported with the following software items:

- LINUX device drivers
- VxWorks device drivers
- User library with examples
- XprsMON and FPGA Built utilities

XprsMON is a Linux application linked with the TOSCA user library which allows the user to interactively perform a set of commands to operate the TOSCA infrastructure:

- Patch, Examine, Deposit & Display operations on Memory and I/O Space references
- Patch, Examine, Deposit & Display operations on VME64x references
- Exercise Interrupts, Global_Time and DMA
- Flash Memory programming (FPGA bit stream remote download)

Debugging & Integration Support

The IPV_1102 unit integrates a local JTAG chain connecting the on-board FPGA and its resources. A standard Xilinx TAP port provides direct access from the Xilinx ISE Design Suite software tool (ChipScope Pro and iMPACT).

Specific software tools are provided to upgrade the FPGA bit-streams in the Serial FLASH devices from the VME64x or PCI Express interfaces.

The P2020 JTAG-COP is made available on a dedicated connector, supporting of the shelf debugging tools.

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FPGA Design Services

IOxOS Technologies provides FPGA design services to support the Virtex-5T central device. Thanks to the full ownership of the TOSCA I VHDL resources, these services guarantees a very high efficiency and performance.

IOxOS Technologies has an in-depth expertise and proven experience in the aerospace domain for military and civil applications (MIL1553, A429, A629, and AFDX) in several industrial form factors (VME64x, VXS, CPCI) and in airborne safety critical applications developed following RTCA DO-254/DO-178B processes.

The sub-contracted engineering services can cover the complete end user application or can be limited to specific areas in order to respect the confidentiality constraints linked to most of the critical applications.

IOxOS Technologies also offers electronic design services for the development of specific customized PMC/XMC IO Modules. Our engineering team has strong experience in high-speed ADC/DAC with high frequency analog front-end sections. IOxOS Technologies also masters the military environmental processes DO-160 and conduction cooled ruggedized implementations (VPX, VXS).

Specifications

Power Consumption (PMC/XMC not plugged)	+5V → 4[A] (VITA 1.7 max 7.5[A] +3.3V → 0.0 [A] (only for PMC/XMC) +12V / -12V (only for PMC/XMC)
Compliance	VME64x VITA 1.1 + VITA 1.5-2003 XMC VITA 42.3
Operating Temperature	0ºC to +55ºC 400 LFM (Commercial) -40ºC to +55ºC 400 LFM (Industrial)
Operating Humidity	10% to 90% non-condensing
Regulatory Compliance	Immunity: EN50082-2 / EN55024 Emission: EN55022 Class A Safety: EN60950

Ordering Information

Article Reference	*Product Description*
IPV_1102-A0	IPV_1102 basic version (P2020 @ 1.2 GHz, Virtex-5T LX30T, and 1 GBytes system memory) enhanced with VME P0 connector
IPV_1102-C0	IPV_1102 basic version (P2020 @ 1.2 GHz, Virtex-5T LX30T, and 1 GBytes system memory)

For IPV_1102 specific options such as FPGA type, System Memory size, and P2020 configurations contact directly with IOxOS Technologies.

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