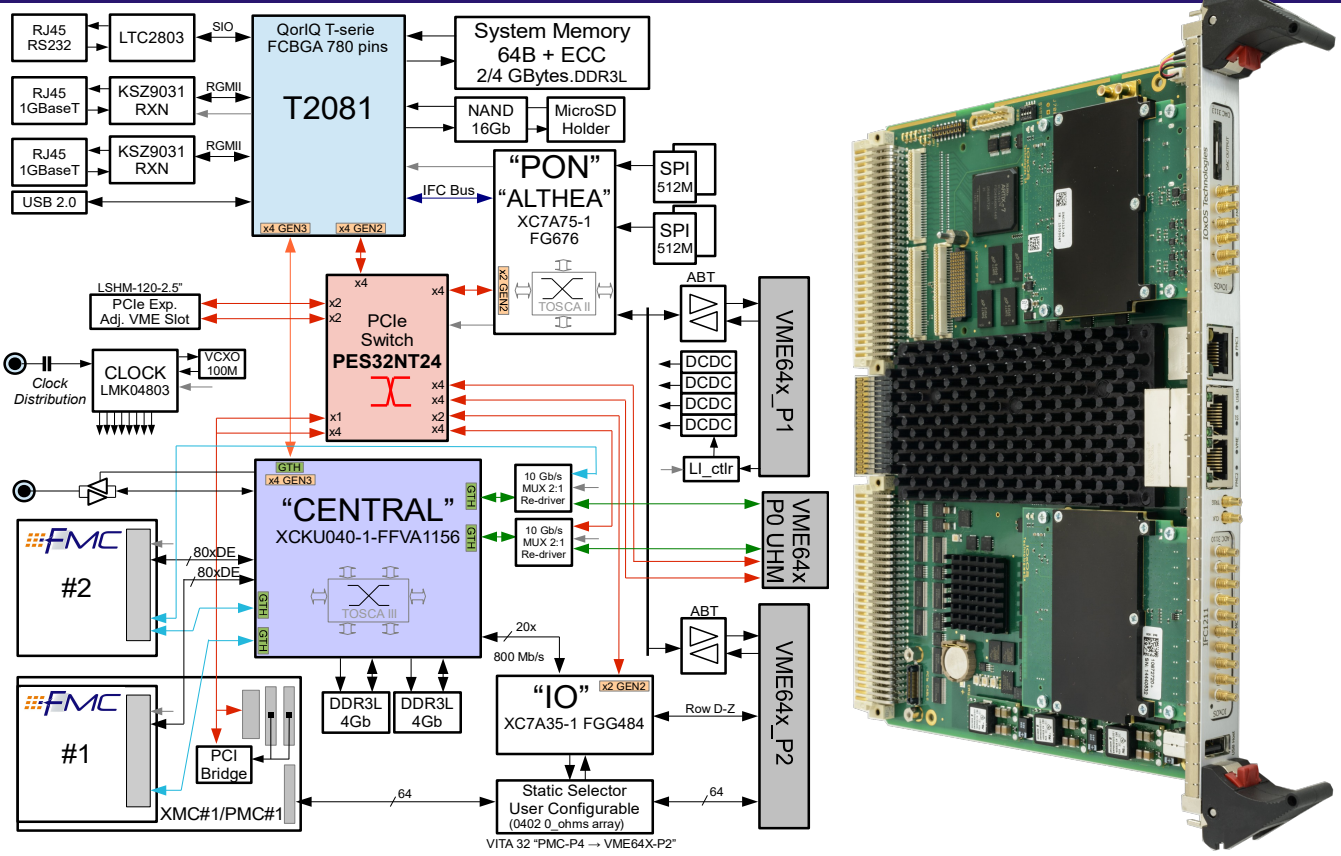
IFC_1211 Single Board Computer

IFC_1211 Intelligent FPGA Controller
T2081 & Kintex UltraScale VME64x SBC

Data Sheet



Key Features

- 6U VME64x Single Board Computer
  - Freescale PowerPC e6500 computing core
  - QorIQ T2081 1.4 (1.8) GHz
  - 2 / 4 GBytes DDR3L System Memory
  - NAND Flash, NOR Flash
  - Dual 10/100/1000 BaseT Ethernet
  - Single RS232
- PCIe GEN2 24-port switch PES32NT24
  - Eight NTB ports
  - Multicast support
  - Embedded DMA Controller
  - SSC / CFC clocking
- Single VITA 42.3 XMC/ PMC Mezzanine
- Dual VITA57.1 HPC FMC Mezzanines
- Quad/Octal Tx/Rx 12.5 Gb/s JESD204B
- UHM VME P0 extension (7 Gb/s)
- VME64x Master/Slave with 2eSST support
- Thermal and Power supplies monitoring
- Xilinx Kintex UltraScale CENTRAL FPGA
- Xilinx Artix-7/ FF484 IO FPGA
- Powered by TOSCA III FPGA Design Kit
- Linux / EPICS / VxWorks BSP

Overview

IOxOS Technologies introduces the IFC_1211, a 6U VME64x highly configurable Single Board Computer featuring embedded FPGA capability and VITA 42.3 XMC, PMC, VITA57.1 FMC I/O expansion slots.

The IFC_1211 is backward compatible with its P2020 based predecessor, the IFC_1210, providing highest computing power with hardware based FPU/ALTIVEC and high performance Xilinx Kintex UltraScale FPGA.

The IFC_1211 integrates the latest generation of Freescale PowerPC QorIQ processors. The T2081 provides quad dual threat core capability running up to 1.8 GHz with medium power operation (~14[W] Typ. @ 1.4 GHz), and is complemented by large DDR3L System Memory (up to 4 GBytes), non volatile memory NOR, NAND and multiple I/O capabilities such as dual 1000 Base-T Ethernet.

The on-board Xilinx Kintex UltraScale FPGA implements a high performance Network on Chip (NoC) switched interconnect. This NoC architecture provides a non-blocking, controlled low-latency and high-throughput bandwidth interface between the data producer and consumer. TOSCA III, a comprehensive FPGA Design Kit developed by IOxOS Technologies, is available for the development and integration of custom applications.

The IFC_1211 features the IOxOS Technologies proprietary PCI Express to VME64x Bridge (code name ALTHEA 7910). This field proven FPGA based solution supports all Master/Slave VME64x modes of operation with Slot_1 System Controller function, and also guarantees the long term availability of the board as a result of not depending on already obsolete third parties VME interfaces.

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Introduction

The IFC_1211 is a HW/SW compatible high-performance upgrade of the widely deployed IFC_1210 P2020/Virtex-6T platform featuring the following major improvements:

- T-series QorIQ up to 1.8GHz with hardware FPU and ALTIVEC units
- Latest Xilinx FPGA generation (Artix-7 and Kintex UltraScale XCKU040)
- PCIe GEN3 direct connection T2081 → XCKU040
- FMC VITA57.1 Multi-Gigabit link up to 12.5 Gb/s with direct support of JESD204B Interface
- Utra low-jitter clock distribution based on LMK04803B with 100MHz VCX0
- User configurable VME_P2 ↔ Jn24 PMC/XMC
- TOSCA III FPGA Design Kit with 128-bit data width
- Dual PMC/XMC carrier expansion on VME adjacent slot
- ALTHEA 7910 VME64x Bridge
- VME P0 with user interface up to 12.5 Gb/s

QorIQ T-Series Computing Core

The IFC_1211 implements a QorIQ T-2081 CPU featuring:

- 1.8 / 1.4 GHz, 4x e6500, 14 to 18 [W]
- 2/(4) GBytes DDR3L-2133 System Memory with ECC
- 128 MBytes emulated NOR Flash Memory (bootable)
- 128 Mbit SPI Serial Flash Memory
- One Micro-SD card holder

The front-panel I/O embeds the following resources:

- Two(2) RJ45, Ethernet 10/100/1000 Base-T
- One RJ45 RS232
- 1 USB 2.0 Host Type A
- Two coax SSMC for external clock reference and/or direct "CENTRAL" connection

Artix-7 "PON" FPGA

The "PON" FPGA, (XC7A75-1-FGG676) implements the following key functions.

- PCIe x2 GEN2 EP ← PES32NT24 Port[3:2]
- Power-up/Cold/Warm RESET sequencer and T2081 configuration
- T2081 IFC Bus Interface for NOR Flash emulation
- "CENTRAL" & "I/O" FPGA configuration from attached SPI Flash Memory and/or under control of UBOOT
- I2C, SMBus, PMBus, SPI, and uWIRE Master Controller
- Low latency direct path (IFC Bus) directly connected to VME64x Master
- ALTHEA 7910 PCI Express to VME64x Bridge

To be fully operational, the T2081 computing core only requires the "PON" FPGA to be configured and functional. "I/O" and "CENTRAL" FPGA can be configured later with bitstream images downloaded from an Ethernet FTP server.

Artix-7 "I/O" FPGA

The "I/O" FPGA, (XC7A35-1-FGG484) is intended to VME64x P2 User I/O Management. Following interfaces are connected to this programmable resource:

- PCIe x2 GEN2 EP ← PES32NT24 Port[3:2]
- High-speed bi-directional link with "CENTRAL" FPGA
- VME_P2 rows D/Z 3.3[V] direct management.
- VME_P2 rows A/C 3.3[V] management through user configurable wiring option.

Kintex UltraScale "CENTRAL" FPGA

The IFC_1211 "CENTRAL" FPGA is allocated to user application, providing FMC VITA57.1 interfacing resources. This FPGA is a major upgrade from the previous family based on Virtex-6T devices, featuring:

- XCKU40-1-FFVA1156 (populated by default) or XCKU35 or XCKU40 (upon request)
- 440K LE and BRAM resources
- PCIe x4 GEN3 EP directly connected to T2081
- PCIe x4 GEN3 EP/RC available on VME_P0 UHS
- Five (5) GTH up to 12.5 Gb/s
  - 2x(1x) GTH to VME_P0 with external 2:1 mux-re-driver DS125MB203
  - 1x(0x) GTH to PCIe Switch 32NT24
  - 2x(3x) GTH to FMC VITA57.1
  - 1x GTH to PCIe x4 GEN3
- TOSCA III FDK with 128-bit NoC non-blocking switch

Two (2) DDR3L Memory parts are directly connected to the "CENTRAL" FPGA, and are fully supported by TOSCA III FDK (2 Bank @ 3.2 GBytes/s with 2/4 IDMA).

PCI Express Centric Architecture

The IFC_1211 PCI Express infrastructure is implemented through a PES32NT24 switch, providing full backward compatibility with the IFC_1210.

- Port[1:0] → PCIe x4 QorIQ T2081
- Port[2] → PCIe x2 "PON" FPGA - ALTHEA 7910
- Port[3] → PCIe x2 "I/O" FPGA
- Port[5:4] → PCIe x4 XMC #1 VITA 42.3
- Port[7:6] → PCIe x1 PMC #1 PCIe-> PCI
- Port[15:8] → PCIe x8, x4, x2, x1 VME64x P0 UHM
- Port[23:16] → PCIe x4, x2, x1 LSHM PCIe Expansion
- Port[23:20] → PCIe x4 "CENTRAL" FPGA GTH224

The UP-stream port and the PCI Express clocking schema is fully configurable through its SMBus or/and a configuration EEPROM. Ports 2, 3, 4 and 5 can be configured in Non-Transparent mode (NTB). Ports [7:4] and [15:8] can be merged to implement PCI Express x8 ports.

PMC / XMC Mezzanine Slot

The IFC_1211 provides one (1) XMC/PMC Mezzanine slot. The PMC slot is controlled by a legacy 32-bit PCI (33/66 MHz) bridged from the PCI Express infrastructure.
The XMC VITA 42.3 slot is controlled by one independent PCI Express GEN2 x4 port.

PCIe XMC/PMC Expansion

The IFC_1211 single XMC/PMC mezzanine resource can be expanded to up to three slots, by attaching the XPM_1262 expansion module, a dual XMC/PMC carrier board.

The XPM_1262 is connected to the IFC_1211 PCI Express infrastructure (through Port[20:16] of the PES32NT24 switch) with a high speed coax flat cable, SAMTEC HLCD, that matches the PCIe GEN2 bandwidth requirements.

The IFC_1211 / XPM_1262 interconnect link includes a dedicated mechanism supporting easy insertion/de-insertion in the VME64x back-plane.

FMC VITA57.1 Carrier

The IFC_1211 is fitted with two (2) VITA 57.1 FMC High Pin Count (HPC) slots. The 2x 160 I/O (LA[33:0], HA[23:0] and HB[21:0]) are directly connected to the Kintex UltraScale "CENTRAL" FPGA. The electrical interface can be defined either as differential (LVDS) or single-ended.

The on-board LMK04803B VCXO clock synthesizer provides both FMC slots with user programmable low-jitter clock sources.

The FMC VITA57.1 high-speed gigabit signaling DP[3:0] is driven by dedicated Kintex UltraScale GTH (up to 12.5 Gb/s) with direct support of JESD204B protocol, a de-facto standard for new generation high-speed ADC/DAC devices.

- FMC#1 DP[3:0] → XCKU040-GTH228
- FMC#2 DP[3:0] → XCKU040-GTH224
- FMC#2 DP[7:4] → XCKU040-GTH225 (optional)

The IFC_1211 implements specific filtering on the FMC power supplies, GND screening and user programmable VADJ DC/DC, to ensure the maximum performance of ADC/DAC FMC for data acquisition.

Central Clock Generation LMK04803B

The ultra low-jitter clock synthesizer LMK04803B is used to generate on-board clock references. This dual PLL device is attached to a low-jitter 100 MHz VCXO, which can be synchronized with an external clock reference available on a front panel SSMC coax connector.

Thanks to its ultra low RMS jitter (~100[fs]), it can be setup to drive directly user programmable clocks dedicated to high-speed ADC/DAC located on VITA57.1 FMC Mezzanine.

- FMC1/FMC2 VITA57.1 CLK2
- FMC1/FMC2 VITA57.1 CLK3
- FMC1/FMC2 VITA57.1 MGTCLK
- "CENTRAL" FPGA XKU040 GTX226
- "CENTRAL" FPGA XKU040 GTX224
- "CENTRAL" FPGA XKU040 GTX228

The PCI Express 100 MHz clock reference is generated by a dedicated XCO source.

VME64x P0 High-Speed Extension

The IFC_1211 VME64x P0 features the new generation of 3M Ultra Hard Metric (UHM) connectors, supporting data rates up to 7 Gb/s. Through these high speed connections, the following resources can be driven through Rear I/O expansion modules:

- Two (2) PCI Express x4 GEN2/GEN3
- Two (2) Kintex UltraScale Quad_GTH
- Twelve (12) GPIO from the "I/O" FPGA

The VME64x P0 UHM links are isolated with DS125BR800A 12.5-Gbps repeaters with Input Equalization.

- The MPR_1260 Multipurpose Rear I/O module, can extend the P0 7 Gb/s connections through PCI Express x4 external cable (copper/optical).

ALTHEA 7910 VME64x Interface

The VME64x interface is implemented using IOxOS Technologies proprietary ALTHEA 7910 solution, an FPGA based PCI Express to VME64x Bridge. Since 2014, the ALTHEA 7910 is marketed and used by relevant VME manufacturers to replace the obsolete TSI148 device. ALTHEA 7910 includes new features such as:

- Embedded SRAM Shared Memory SMEM 64K/128K
- Direct IDMA PCIe-VME64x without intermediate copy in SMEM
- Message Passing FIFO and Semaphores
- VME A24, A16 Slave windows mapping
- Integration of TSI148 specific functions

In addition, the IFC_1211 implements a direct path (IFC Bus) between the T2081 and the ALTHEA's VME64x Master interface, providing very fast low latency CPU single-beat READ transactions. CPU single-beat WRITE transactions are also posted on this direct path.

VME P2 A/C → Jn14

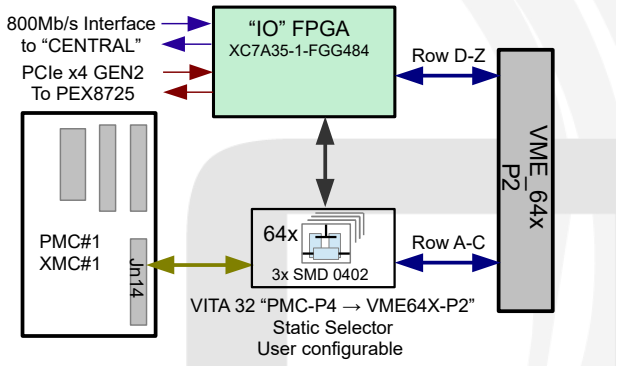
VME P2 rows A&C are wired to PMX/XMC#1 Jn24 through an array of 64 groups of three (3) small resistors (0402). This array can be populated to enable:

(a) Direct electrical connection between P2 ↔ Jn14 including "I/O" FPGA I/O resources (default)

(b) Direct electrical connection between P2 ↔ Jn14

(c) Separated connection including "I/O" FPGA I/O resources

By default (a), the SMD 0402 array is populated with 0 ohms resistors. Other configurations, such as AC coupling or serial termination, can also be built on each array.



TOSCA III FPGA Design Kit

Conventional design kits offer a set of IP Cores along with implementation examples. IOxOS Technologies goes one step further releasing the TOSCA III FPGA Design Kit, a comprehensive system design environment that covers all the path, from the SW application to the FPGA user code.

The TOSCA III FPGA Design Kit is delivered with full VHDL source code together with a set of test-benches and Bus Functional Models (BFM) to set up a complete VHDL simulation environment for functional verification purposes.

The TOSCA III architecture is based on a PCI Express switch centric structure implementing a memory mapped model with segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane).

The TOSCA III FPGA Design Kit enhances the versatility of the IFC_1211 solution, providing the user with a powerful tool for the implementation and integration of custom applications within the IFC_1211 on-board Kintex UltraScale FPGA.

To match PCIe GEN3 performance requirements, the embedded NoC switch is enhanced to support 128-bit data paths.

TOSCA III FDK is fully integrated with Xilinx CAE Tools (VIVADO 2015.2 and later).

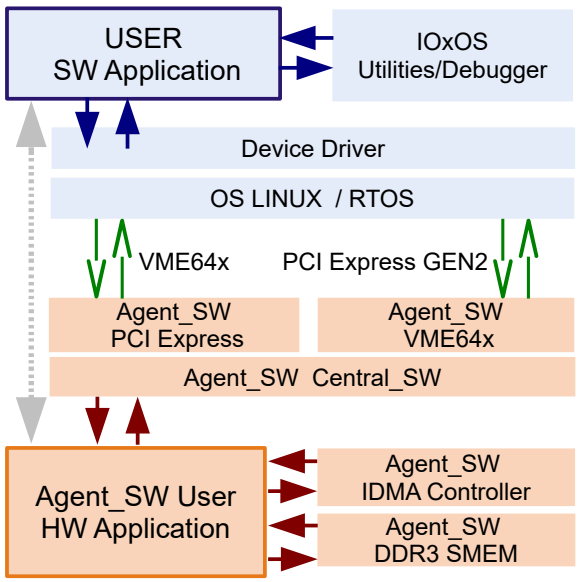
XUSER Specific Applications

The TOSCA III infrastructure is backward compatible with TOSCA II FDK used with the IFC_1210. This means that all XUSER specific applications designed for the IFC_1210 Single Board Computer can be used within the new IFC_1211 TOSCA III environment.

Embedded Health Monitor

The IFC_1211 monitors several physical parameters thanks to its multiple on-board sensors:

- Temperature Monitoring (ambient & junction)
- Input Voltage/Current (from VME64x back-plane)
- Local DC/DC parameters through local PMBus



Software Support

The IFC_1211 is supported with the following software items:

- IOxOS XprsMON with C user's library
- LINUS ELDK distribution
- LINUX device drivers
- Wind River VxWorks with BSP extension specific

Environmental Specifications

Power (estimated) (No PMC, XMC, FMC)	+5V →6[A] (VITA 1.7 max 7.5[A]) +3.3V → 3[A] (VITA 1.7 max 11.2[A]) +12V / -12V (Not used on-board)
Compliance	VME64x VITA 1.1 + VITA 1.5-2003 XMC VITA 42.3 FMC VITA 57.1
Operating Temperature	Commercial: 0°C to +55°C 400 LFM Industrial: -20°C to +55°C 400 LFM
Regulatory Compliance	Immunity: EN50082-2 / EN55024 Emission: EN55022 Class A Safety: EN60950

Ordering Information

Article Reference	*Product Description*
IFC_1211-A0	IFC_1211 T2081 1.4 GHz, XCK040-1 CENTRAL FPGA
XPM_1262-A0	Dual XMC/PMC Expansion Carrier

For IFC_1211 specific options, such as "CENTRAL" FPGA type and System Memory size, please contact directly IOxOS Technologies.

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