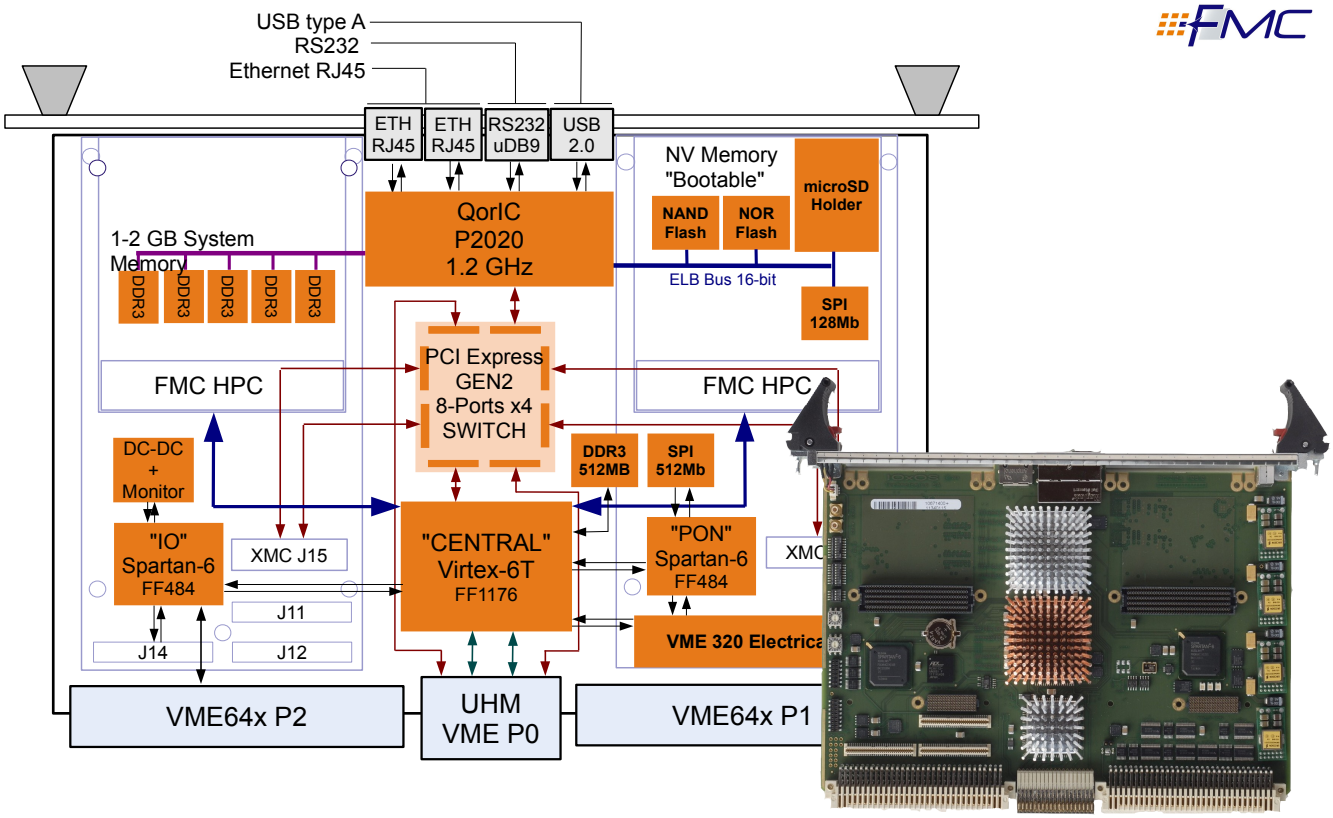
IFC_1210 - Intelligent FPGA Controller P2020 VME64x Single Board Computer

Data Sheet IFC_1210



Features

- 6U VME64x Single Board Computer
- Freescale PowerPC P2020 computing core
  - QorIQ P2020 1.2 GHz
  - 1 or 2 GBytes DDR3 System Memory
  - NAND Flash, NOR Flash
  - Dual 10/100/1000 BaseT Ethernet
  - Single RS232
  - USB 2.0 Host Controller
- High performance PCIe G2 8-ports switch
  - Multiple NTB ports
  - Multicast support
  - SSC / CFC clocking
- Dual VITA 42.3 XMC Mezzanine
- Single IEEE P1386.1 PMC Mezzanine
- Dual VITA57 HPC FMC Mezzanine
- UHM P0 extension (7 Gb/s)
- VME64x Master/Slave with 2eSST support
- Multiboard time synchronization
- Thermal and Power supplies monitoring
- Xilinx Virtex-6T/FF1156 CENTRAL FPGA
- Xilinx Spartan-6/ FF484 IO FPGA
- Powered by TOSCA II FPGA Design Kit
- Linux / VxWorks BSP

Overview

IOxOS Technologies introduces the IFC_1210, a 6U VME64X highly configurable Single Board Computer with embedded FPGA capability and VITA 42.3 XMC, PMC, VITA57 FMC slots. The IFC_1210 is built around a high performance switched PCI Express GEN2 architecture providing low latency and high bandwidth extension capability.

The IFC_1210 is a general purpose high-capacity FPGA platform associated with a high-performance dual core PowerPC. It is well adapted for complex real-time applications and sophisticated data acquisition.

The IFC_1210 integrates the latest generation of Freescale PowerPC QorIQ processors. The P2020 provides dual-core capability running at 1.2 GHz with low power operation (< 8[W] Typ.). It is implemented with large DDR3 System Memory (up to 2 GBytes), non volatile memory NOR, NAND and multiple IO capabilities as dual Gigabit Base-T Ethernet .

The on-board Xilinx Virtex-6T FPGA implements a high performance PCI Express centric Network on Chip (NoC) switched interconnection. This NoC architecture provides a non-blocking, controlled low-latency and high-throughput bandwidth interface between the data producer and consumer.

The VME64x interface, which is also integrated in the FPGA, is implemented with a direct transparent low latency PCI-Express / VME64X bridge. It supports all Master/Slave VME64x modes of operation with Slot_1 System Controller.

TOSCA II, a comprehensive FPGA Design Kit developed by IOxOS Technologies, is available for the implementation of custom applications.

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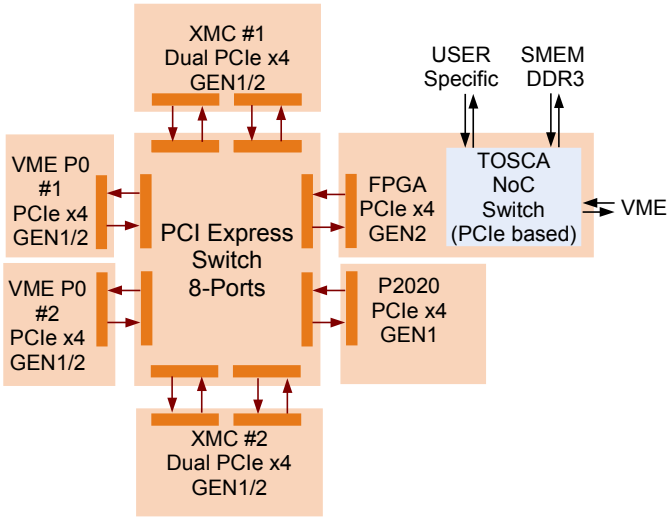
Introduction

The IFC_1210 platform has been designed to support high performance computing in scientific and aerospace real-time applications. The main goal is to provide the key features to support these high demanding applications

- Multi-core PowerPC (P2020) with RT OS support
- High-performance Xilinx Virtex-6T FPGA embedding DSP computing support
- Standard application customization with XMC, PMC and FMC (VITA57) mezzanine slots
- Standard real-time interconnect infrastructure of several Gigabyte/s (PCI Express GEN2)
- External expansion capability to build large systems

PCI Express Centric Architecture

The IFC_1210 is built around the latest generation of PCI Express GEN1/GEN2 non-blocking switches, providing eight (8) PCI Express x4 GEN1/GEN2 ports.



The eight (8) PCI Express x4 ports are mapped as follows:

Port_0	P2020 Central PowerPC Microprocessor
Port_1	Virtex-6T FPGA (VME64x, DDR3, USER areas)
Port_2	VME64x P0 UHM
Port_3	VME64x P0 UHM
Port_4	XMC #1 VITA 42.3
Port_5	XMC #1 VITA 42.3
Port_6	XMC #2 VITA 42.3
Port_7	XMC #2VITA 42.3

The Upstream port (connected to the Root Complex) and the PCI Express clocking schema (local CFC or external SCC/CFC) are fully configurable.

Ports 2, 3, 4, 5, 6, 7 and 8 can be configured in Non-Transparent mode (NTB). Ports {2:3}, {4:5} and {6:7} can be merged to implement PCI Express x8.

The PCI Express topology is naturally extended inside the FPGA fabric by means of TOSCA II's native Network on Chip (NoC) non-blocking switch. This provides an unified PCI Express centric architecture.

Eight Port PCI Express Switch

The non-blocking eight (8) port PCI Express switch supports advanced modes of operation such as:

- PCI Express 2.1 compliance (2.5 Gb/s or 5.0 Gb/s)
- 256 Gbps aggregate switching capacity
- Low latency cut-through architecture with advanced QoS support
- Up to eight (8) NT endpoint with 6 BARs per NT
- Multicast capability over the eight (8) ports, including the NT
- Dynamic port reconfiguration (Upstream, Downstream and NT Bridge)
- Embedded dual DMA controller with link list capability
- Per lane SERDES configuration (De-emphasis, Receive equalization and Drive strength)
- Automatic lane reversal and link width negotiation
- Flexible port clocking mode

External PCI Express Expansion

The onboard IFC_1210 PCI Express network can be expanded externally thanks to the following IO capabilities:

- XMC VITA 42.3. Four (4) PCI Express x4 External Cabling (XMC_3105)
- VME P0 UHM connector. Two (2) PCI Express x4 External Cabling or CX4 electrical/optical

This expansion capability allows to build a local high-performance, memory mapped sub micro-second real-time network interconnecting multiple IFC_1210 together or high performance multi-core based workstations.

P2020 Computing Core Resources

The PowerPC P2020 microprocessor is supported by the following memory resources. All non-volatile resources can be statically selected as Bootable.

- 1 or 2 GBytes DDR3-600 System Memory
- 256 MBytes NAND Flash Memory with ECC
- 16 MBytes NOR Flash Memory
- 128 Mbit SPI Serial Flash Memory

The P2020 PCI Express port can be configured as Root Complex (RC, which manages the local PCI Express enumeration) or as End Point (EP).

P2020 IO Resources

The P2020 provides the following IO on the front panel:

- Two (2) RJ45, Ethernet 10/100/1000 Base-T
- One (1) µDB9, RS232
- One (1) Type A USB 2.0 Host Adapter
- JTAG COP debugging socket (on-board access only)

Additional Resources

- Quad frequency Programmable VCXO
- Dual Hot swap controller
- PCI Express / PCI bridge

VME64x Legacy Interface

The Central Virtex-6T FPGA embeds a proprietary IP Core providing a complete Master/Slave VME64x interface. Thanks to the direct PCI Express to VME64x bridge (with no intermediate PCI Bus), it provides a very low latency access. The electrical interfacing is based on VME320 ETL technology, supporting both full speed 2eSST and 2eVME protocols.

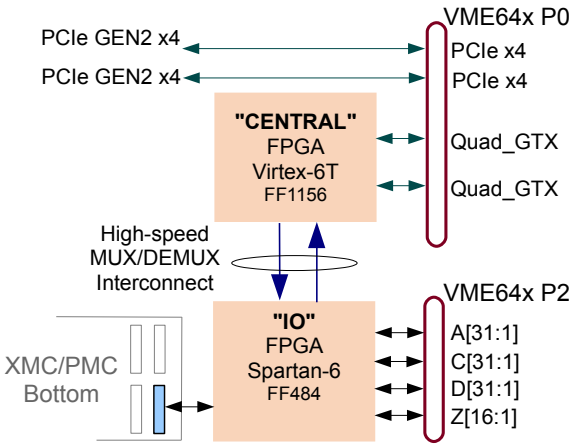
The VME Slave interface implements the legacy VME/VME64 addressing configuration with static switches and/or VME64x CR/CSR. The VME Slave handles all addressing modes including 2eVME and 2eSST. A dedicated MMU scatter-gather allows to redirect the VME across the PCI Express infrastructure.

The VME Master interface, driven by the internal FPGA infrastructure also supports all VME addressing modes, including 2eVME and 2eSST. Under specific control registers it is capable to issue Read-Modify-Write and ADO/ADOH atomic transactions.

In addition, the VME Master embeds a complete VME Slot_1 function, Interrupt Generator/Handler and a global time synchronization (< 0.1 [us]) distribution over the back-plane.

VME64x P2 User IO

The VME P2 User IO (rows A & C / 64 signals 32+32) and the (rows D & Z / 48 signals 32+16) are directly connected to the Spartan-6 IO FPGA. The VME P2 IO signaling is legacy LVTTL.



VME64x P0 High-speed Extension

The IFC_1210 VME64x P0 features the new generation of 3M Ultra Hard Metric (UHM) connectors, supporting data rates up to 5 Gbps. Through theses connections, the following PCI Express GEN2 and Virtex-6T GTX transceivers resources can be extended through rear IO extension modules:

- Two (2) PCI Express x4 GEN2
- Two (2) Virtex-6T Quad_GTX
- Sixteen (16) GPIO from the IO FPGA Spartan-6

The MPR_1260 Multi-purpose Rear IO module, can extend the P0 Gbit connections through external cabling (PCI Express External cable or CX4 electrical/optical)

PMC / XMC Mezzanine

The IFC_1210 provides two (2) XMC Mezzanine slots and one (1) PMC mezzanine slot for custom expansions.

The PMC slot is controlled with legacy 32-bit PCI (33/66 MHz) bridged from the PCI Express infrastructure. The PMC User IOs (Jn14 / Jn24) are directly routed to the Spartan-6 IO FPGA.

Both XMC VITA 42.3 slots are controlled with two independent PCI Express GEN2 x4 interfaces which can be merged to form a single PCI Express GEN2 x8.

Both XMC slots can be equipped with the XMC_3105 board, a Dual PCI Express External Cable adapter which allows high-performance PCI Express expansion outside the IFC_1210.

FMC VITA57

The IFC_1210 provides two VITA 57 FMC with HPC (High Pin Count). The 160 IO of the two FMC are directly connected to the Virtex-6T “CENTRAL” FPGA. The electrical interface can be defined as differential or single-ended.

The VITA57 FMC are usually dedicated to analog conversion (ADC, DAC, TDC, …) requiring a low noise environment. The IFC_1210 implements dedicated filtering on the FMC power supplies to fulfill this requirement.

Spartan-6 “IO” FPGA

A Xilinx Spartan-6 “IO” FPGA is dedicated for the VME P2 User IO management. The “IO” FPGA is connected to the PMC Jn14 (64 signals) and to the VME P2 rows A, C, D and Z. The “IO” FPGA is also connected to the “CENTRAL” FPGA through bi-directional source synchronous interface (2 x 16-bit data + clock). Back-end multiplexor / demultiplexor are supplied for both FPGAs.

Virtex-6T “CENTRAL” FPGA

The IFC_1210 Xilinx Virtex-6T “CENTRAL” FPGA can be selected across the whole Virtex-6T device family.

- CX130T, CX195T and CX240T
- LX130T, LX195T, LX240T and LX365T
- SX315T and SX475T

The IFC_1210 features a high-capability DCDC dedicated to the on-board FPGA which is able to support any device from the Xilinx Virtex-6T family.

Two (2) 128 Mbit SPI Flash EPROM devices, controlled by the Power ON “PON” FPGA, are used to store up to four FPGA configuration bit-streams. Both SPI Flash devices are used in parallel by the configuration FSM, achieving ultra fast configuration data rates (800 Mbps).

Two (2) DDR3 Memory devices are connected to the Virtex-6T “CENTRAL” FPGA. The DDR3 IP Core memory controller which provides the complete control of the DDR3 devices is part of the TOSCA II FPGA Design Kit (1 Bank @ 1.6 GBytes/s with 2 or 4 DMA channels).

Other functions such as the I2C and SPI interfaces, GPIO management, Power-ON FSM controller, and power supply monitoring, are integrated within the Virtex-6T Central FPGA firmware developed with the TOSCA II FPGA Design Kit.

Power Supplies

The IFC_1210 implements latest generation of high efficiency DCDC converters for on-board high-current devices. These DCDC are controlled with a dedicated PMBus (I2C).

Through this PMBus interface, the following DCDC parameters can be controlled / monitored:

- Phase synchronization
- Output voltage adjust
- Output voltage and current monitoring
- Over/Under value tracking

Monitoring

The IFC_1210 can measure several physical parameters thanks to extensive on-board sensors:

- Temperature Monitoring (ambient & junction)
- Input Voltage (from VME64x back-plane)
- Input Current (from VME64x back-plane)

TOSCA II FPGA Design Kit

Conventional design kits offer a set of IP Cores along with implementation examples. IOxOS Technologies goes one step further releasing the TOSCA II FPGA Design Kit, a comprehensive system design environment that covers all the path, from the SW application to the FPGA user code.

The TOSCA II FPGA Design Kit can be delivered with full VHDL source code together with a set of test-benches and Bus Functional Models (BFM) to set up a complete VHDL simulation environment for functional verification purposes. This simulation environment is supported by the main HDL simulation tool vendors.

The TOSCA II architecture is based on a PCI Express switch centric structure implementing a memory mapped model with segregated I/O Space (CONTROL Plane) and Memory Space (DATA Plane).

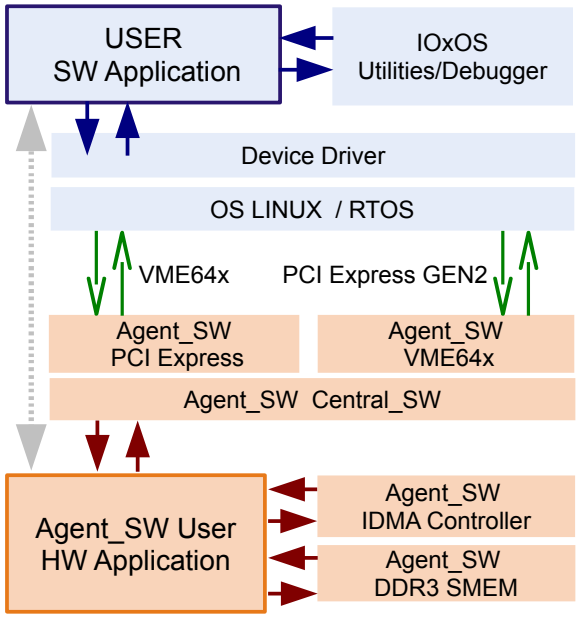
The TOSCA II FPGA Design Kit enhances the versatility of the IFC_1210 solution, providing the user with a powerful tool for the implementation and integration of custom applications within the IFC_1210 on-board Virtex-6T FPGA.

Debugging & Integration Support

The IFC_1210 unit integrates a local JTAG chain connecting the on-board FPGA and its resources. A standard Xilinx TAP port provides direct access from the Xilinx ISE Design Suite software tools (ChipScope Pro and iMPACT).

Specific software tools are provided to upgrade the FPGA bit-streams in the Serial FLASH devices from the VME64x or PCI Express interfaces.

The P2020 JTAG-COP is made available on a dedicated connector, supporting of the shelf debugging tools.



Software Support

The IFC_1210 is supported with the following software items:

- IOxOS XprsMON with C user's library
- LINUX device driver
- Wind River VxWorks with BSP extension specific

Specifications

Power (estimated) (No PMC, XMC, FMC)	+5V → 4[A] (VITA 1.7 max 7.5[A] +3.3V → 3[A] (VITA 1.7 max 11.2[A] +12V / -12V (Not used on-board)
Compliance	VME64X VITA 1.1 + VITA 1.5-2003 XMC VITA 42.3 FMC VITA 57.1
Temperature Operating	0ºC to +55ºC 400 LFM (Commercial) -20ºC to +55ºC 400 LFM (Industrial)
Regulatory Compliance	Immunity : EN50082-2 / EN55024 Emission : EN55022 Class A Safety : EN60950

Ordering Information

Article Reference	*Product Description*
IFC1210-A0	IFC_1210 with dual XMC slots and dual FMC HPC slots
IFC1210-B0	IFC_1210 with dual XMC slots and no FMC

For IFC_1210 specific options such as FPGA type and System Memory contact directly with IOxOS Technologies.

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The IFC_1210 has been developed in collaboration with the Paul Scherrer Institute (PSI) in Villigen (Switzerland)

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