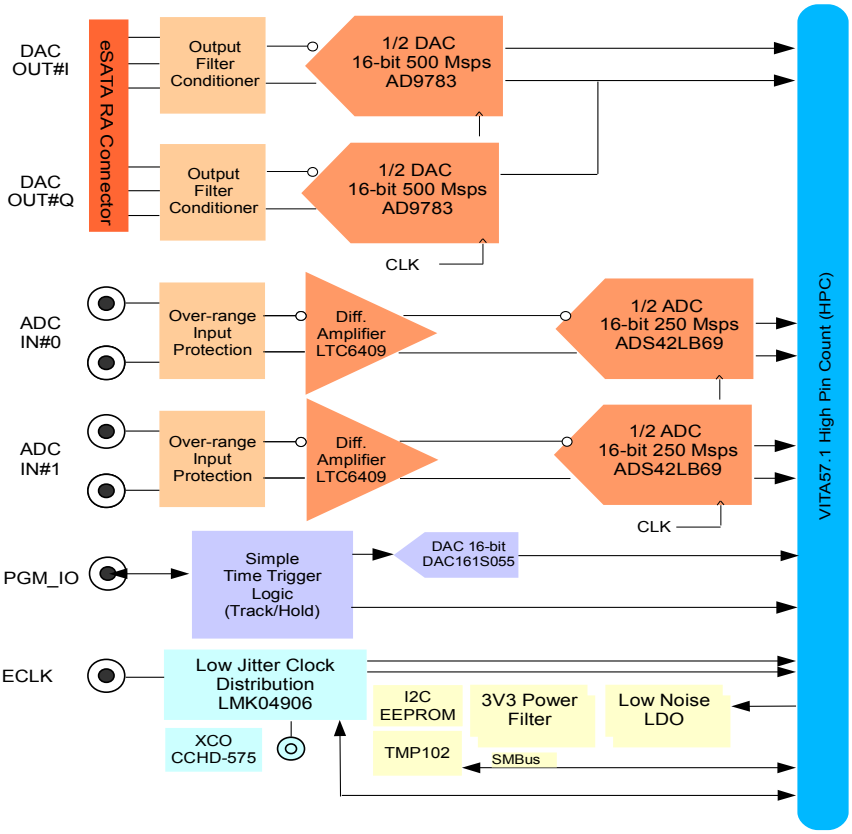
DAC_3113 – Dual 16-bit DAC + Dual 16-bit ADC Data Sheet

FMC Mezzanine Board — **DAC_3113_DS_A1**



Key Features

- Single width FMC VITA 57.1-2008
  - HPC 400 pins connector
  - Six (6) SSMC front panel connectors
  - One (1) eSATA II right angle connector
  - 9[W] typical power consumption
- Dual channel 16-bit/250 (500) Msps DAC
  - Analog Devices AD9783 16-bit / 500Msps
  - 2x 50 Ω DC coupled Differential outputs (eSATA)
  - Source current 10 to 30[mA] full range
  - 20 MHz 6th order Bessel output filter
  - Common mode adjust
- Dual channel 16-bit/250 Msps ADC
  - TI ADS54LB69
  - Differential 50 Ω Inputs with software selectable differential /single-ended modes
  - DC coupling with preamplifier LTC6409
- High-end programmable clock tree distribution
  - TI LMK04906 (dual PLL)
  - Low jitter clock distribution <100[fs]
  - On-board ultra-low noise oscillator (VCXO/XCO)
  - External SSMC clock reference
- XILINX Virtex 6/7 FPGA VHDL Design Kit
- LINUX Software Library

Overview

IOxOS Technologies releases the DAC_3113, a VITA 57.1-2008 form factor module featuring dual 16-bit 250Msps ADC and dual 16-bit 250/500Msps DAC.

The DAC_3113 is the third member of IOxOS Technologies' FMC VITA 57.1 data acquisition product line integrated by the ADC_3110 (16-bit 250Msps ADC with AC coupling), and the ADC_3111 (16-bit 250Msps ADC with DC coupling).

The dual 16-bit 250Msps ADC channels are implemented with a DC coupled front-end preamplifier, through four (4) SSMC connectors. The analog ADC inputs can be configured to operate in single-ended or differential mode.

The dual 16-bit 250/500Msps DAC channels are implemented in differential mode with outputs routed to a eSATA II differential connector. The DAC AD9783 output stage is powered with ultra low-noise power supplies built with a 2 level cascaded LDO. A 6th order Bessel passive filter is implemented in both DAC output paths.

The on-board clock tree is implemented with a high-precision low-jitter low-phase noise clock fully programmable controller LMK04906. Input clock reference can be selected either from the on-board XCO or from the front panel SSMC CLKREF.

A user programmable GPIO SSMB can also be defined as External TRIGGER, GATE, CLOCK replication or any other user programmable function.

The DAC_3113 targets the following applications:

- Test measurement equipments
- Scientific / Physics experiments
- LLRF control loop

IOxOS Technologies SA - Chemin des Fontenailles 4, 1196 Gland, Switzerland
Tel : +41 22 364 76 90 Fax: +41 22 364 76 94 www.ioxos.ch

Introduction

The DAC_3113 is a FMC VITA57.1 module featuring a dual channel high precision 16-bit DAC complemented with a dual channel 16-bit 250Msps ADC.

Differential DAC

The dual channel DAC is implemented with an Analog Devices AD9783 device. This DAC provides a low pipeline (7 clock cycles) data interface operating up to 500 Msps.

The dual differential DAC outputs implement 50 ohms source termination, converting the DAC current source (up to 30[mA] full scale) to DC voltage outputs.

To provide optimal differential integrity, the DAC output signaling is routed to an eSATA II connector, with dual shielding level.

An optional specific circuitry, built with two 16-bit DACs, allows to compensate from 0 to -30[mA] the inherent common mode due to the DAC current source. This circuitry is independent for both channels.

A configurable 6th order Bessel filter is implemented at the output of each channel. This filter has a Fc = 20 MHz by default.

Differential ADC

The DAC_3113 also implements two 16-bit ADC channels with a DC coupling input stage that can operate in differential or single-ended mode.

INPUT Amplifier mode	Gain	IN range	IN max	Z_{IN}
Differential INPUT	2.2 (6.8 dB)	+/- 0.5V differential mode -0.5V to +1.0V common mode	+/- 2.0V	100 Ω diff.
POS Single ended INPUT	2.0 (6.0 dB)	+/- 0.5V	+/- 2.0V	50 Ω
NEG Single ended INPUT	-2.0 (6.0 dB)	+/- 0.5V	+/- 2.0V	50 Ω

Clock Distribution

The on-board clock distribution is implemented with a low-noise low-jitter dual PLL clock driver, the TI LMK04906, with clock jitter < 100[fs]. The LMK04906 clock source can be selected from :

- Front panel AC coupled SSMC "CLKREF"
- On-board ultra-low phase noise oscillator (Crystek CCHD-575)

Six (6) output clocks, with programmable delay in steps down to 25[ps], are supplied to the DAC AD9783 device, to the ADC ADS42LB69 and to the Trigger Time Stamping logic.

The LMK04906 incorporates a uWIRE Bus and is fully configurable from the VITA57.1 carrier board FPGA.

Power Supplies

The DAC_3113 on-board power supplies are locally built with low noise DCDC and LDO devices.

A bulk DCDC generates a local 4.3[V] from the FMC VITA57.1 P3V3 power supply. This local 4.3[V] is used as source for three low-noise LDOs, providing the following voltages:

- Low noise 3.3[V] for AD9783 devices
- Low noise 1.8[V] for AD9783 devices
- Low noise 3.3[V] for LMK04906 and VCXO/XCO

The on-board negative power supplies are also generated from a DCDC to properly feed the low-noise LDO.

DCDC operating frequency can be synchronized by the carrier board. One low noise LDO is directly powered by FMC VADJ and generates a local 1.8[V] dedicated to ADS42LB69 digital read-out section (LVDS).

Other Resources

The DAC_3113 embeds a 256K EEPROM and a temperature sensor TMP102, both connected on the VITA57.1 native SMBus.

TOSCA II FPGA Design Kit

IOxOS Technologies has developed TOSCA II, a complete FPGA Design Kit optimized for XILINX Virtex 6/7 FPGA devices using VHDL as description language, to interface the DAC_3113 with the carrier's FPGA. In addition, the design environment includes the following functions:

- General DAQ Management
- AD9783 Data generation up to 500Msps
- ADS42LB69 Data Acquisition up to 250Msps
- Arbitrary Waveform Generator
- SPI Bus controller for ADS42LB69, AD9783
- uWIRE Bus controller for LMK04906
- Trigger Time Tagging at 250[ps] resolution
- GPIO, LED, and basic control functions

Firmware/Software Support

IOxOS Technologies proposes a development platform made of a high-end VME64x Virtex-6T based FMC carrier, the IFC_1210, TOSCA II design environment including FPGA firmware (VHDL sources and binary files), LINUX libraries and data acquisition design examples.

This comprehensive tool allows the implementation of IFC_1210 based systems featuring the DAC_3113 modules, through a fully functional application example.

An EPICS driver for this development platform is also available. EPICS drivers for IFC_1210 were developed by the Paul Scherrer Institute (PSI), and are released upon request under an open source license (http://epics.web.psi.ch/).

IOxOS Technologies also provides design services for the development of custom applications for XILINX and ALTERA based systems.

Ordering Information

Article Reference	*Product Description*
DAC_3113-A0	Dual 16-bit DAC + Dual 16-bit ADC
FDK_3113	FPGA VHDL Reference Design Kit

For other configurations please contact IOxOS Technologies

4, chemin de Fontenailles
1196 Gland
SWITZERLAND
tel: +41 (0)22 364 76 90

Email: info@ioxos.ch