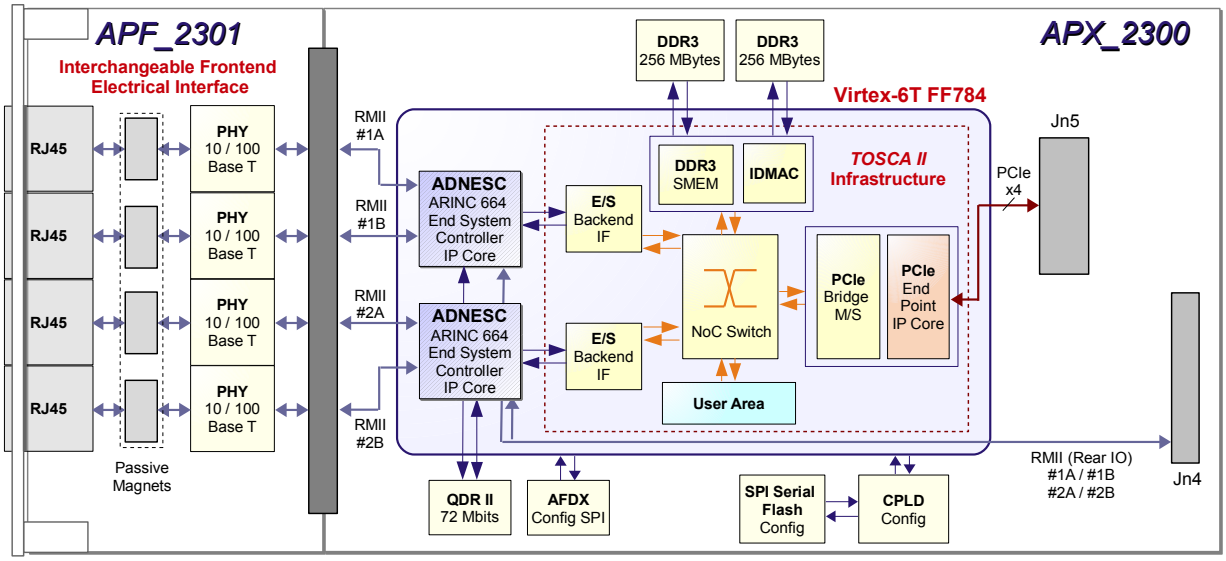
APX_2300 – 2 x AFDX E/S Controller XMC Mezzanine Board

Data Sheet APX_2300_DS_A2



Key Features

- Built on latest Xilinx Virtex-6T technology with PCI Express GEN2 embedded support
- XMC VITA 42.3 form factor supporting PCI Express GEN2 x4, x2 and x1
- Up to Two (2) Dual Redundant ARINC 664 Channels
- Embedding High-performance ADNESC ARINC 664 End System Controller:
  - ✔ Performance in reception of 100%
  - ✔ No jitter in transmission
  - ✔ No limit for number of Virtual Links in transmission (depends on available memory size)
  - ✔ Up to 2048 Virtual Links in reception
- Built-in Safety Monitoring and Failure Detection Mechanisms
  - SECDED for logic error detection and correction
  - Continuous memory integrity checking
  - BIST capability
- On-board SPI Flash to store several ARINC 664 End System Configuration Tables
- Standard air cooled (0°C to 70°C) version

Overview

IOxOS Technologies introduces the APX_2300, an XMC form factor board featuring up to two (2) dual redundant ARINC 664 End System controllers fully implemented in hardware.

The two (2) dual redundant ARINC 664 channels are available in the front panel connectors provided by the APF_2301, an interchangeable frontend electrical module, which also implements the PHY transceivers and passive magnetic devices to enable the network interface. These ARINC 664 channels are also directly routed to the Jn4 PMC connector to increase the versatility and integration level of systems using this XMC module.

The ARINC 664 protocol stack is fully implemented in hardware, by means of IOxOS Technologies' ADNESC (ARINC 664 End System Controller) solution, an IP Core fully developed in VHDL which provides the highest performance and interface flexibility along with additional ARINC 664 testing capabilities such as error injection, monitoring ports and additional time-stamping.

The APX_2300 targets the following applications:

- Aerospace integration rig systems
- Flight simulators
- ARINC 664-based test equipments

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Introduction

IOxOS Technologies introduces the APX_2300, an XMC form factor board featuring up to two dual redundant ARINC 664 End System controllers, targeting aerospace integration rig systems, flight simulators and test equipments.

ARINC 664 End System IP Core

The ARINC 664 protocol stack is fully implemented in hardware by means of IOxOS Technologies' ADNESC (ARINC 664 End System Controller) solution, an IP Core fully developed in VHDL featuring:

- ARINC 664 End System Compatibility: Compliant with main aircraft manufacturers specification
- Airworthiness: IP Core development process fully compliant with RTCA DO-254 DAL A
- Target Device Independence: Targets multiple FPGA and Structured ASIC devices
- Growing Capability: High modularity for future "fieldbus" oriented functionality

The End System is seen by the application as a memory-mapped buffer to post/read the message payload to/from a selected port. This approach dramatically unloads most of the end user tasks at system level.

The ARINC 664 End System IP Core implements additional capabilities such as error injection (performed at ARINC 664 protocol stack level to provide more realistic scenarios for test), monitoring ports and additional time-stamping.

FPGA Based Solution

The full solution (ARINC 664 End System controllers, XMC PCI Express support and shared memory controllers) is built in a Xilinx Virtex-6T FPGA, using IOxOS Technologies proprietary *TOSCA II* FPGA Design Kit, a comprehensive design environment based on a Network on Chip (NoC) PCI Express switch-centric architecture. All the FPGA components are tightly coupled, including an embedded user area reserved for custom applications.

This approach allows easy scalability and growing capabilities while improving the overall performance. The backend interface which controls each ARINC 664 End System can also be modified to enable enhanced End System management features such as ARINC 664 Port Subscriber Services.

The APX_2300 is ready to be equipped with several Virtex-6T devices in FF784 package (LX75T, LX130T, LX195T and LX240T), depending on the extra logic resources requirements for custom applications.

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ARINC 664 Support

The embedded ADNESC ARINC 664 End System Controller provides the following features:

- FPGA based solution with growing capability for future "fieldbus" oriented functionality
- Up to two (2) dual redundant ARINC 664 channels available in the front panel connectors or through the Jn4 PMC connector
- Fully compliant with main aircraft manufacturers specification
- Performance in reception of 100% (full support of back-to-back frames at maximum throughput)
- Isochronous Traffic Scheduling to avoid Jitter in Transmission
- No limit for Virtual Links in transmission (depends on memory size allocated)
- Up to 2048 Virtual Links in reception
- Up to 72 Mbits of QDRII memory
- On-board SPI Flash to store several ARINC 664 E/S Configuration Tables
- Physical Layer (PHY) interfaced through RMII for 10 / 100 BaseT Ethernet support
- Interchangeable frontend electrical interface to adapt to different ARINC 664 network connectors (RJ45 by default). This frontend also provides the PHY transceivers and the passive magnetic devices

Shared Memory

The APX_2300 implements two (2) independent banks of 256 MBytes of DDR3 with an PCI Express-optimized DMA controller embedded in the Virtex-6T FPGA.

Software Support

A device driver for Windows and Linux is supplied with a comprehensive set of tools for debugging, FPGA bit-stream upgrading, on-board chained DMA control and PCI Express mapping.

The APX_2300 is ready to support specific ARINC 664 network test and analysis tools.

Ordering Information

Article Reference	*Product Description*
APX2300-A0	Dual ARINC 664 E/S Controller XMC mezzanine basic version (Virtex-6T LX130T / 512 MBytes DDR3 / 18 Mbit QDR II)
APF2301-A0	Dual ARINC 664 frontend signal conditioning unit