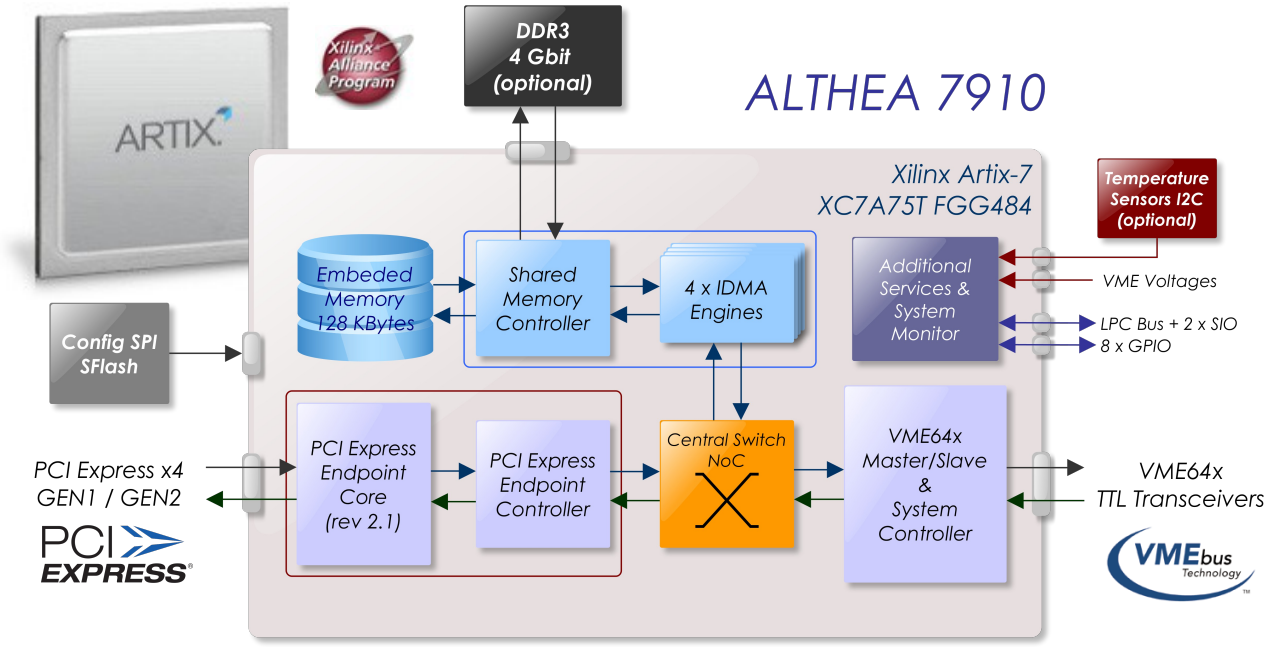
ALTHEA 7910
PCI Express to VME64x Transparent Bridge — Data Sheet



Key Features

- Transparent PCI Express - VME64x Master / Slave Bridge with embedded chained DMA and local shared memory
- Single chip, low power solution (< 1.5[W])
- Network on Chip (NoC) based architecture
- True PCI Express End Point x4 GEN1/GEN2 (v 2.1)
- Targets Xilinx Artix-7 XC7A75T device in FGG484 package
- Available in Commercial, Industrial and Military (XQ7A100T device) temperature ranges
- Higher performance compared to legacy ASIC solutions
- Low Read latency (PCI Express-VME64x)
- VME 3 and 5 rows support
- Little / Big endian conversion by hardware
- High performance DMA (>1'600 MBytes/s with PCI Express GEN2)
- IO Space for CSR mapping
- Programmable Memory Space window size (Prefetchable and Non-Prefetchable)
- INgress MMU based IO scatter-gather on PCI Express and VME Slave ports
- VME Address CFG, A16, A24, A32, ADO, and ADOH
- VME Data D08, D16, D32, BLT32, MBLT64, 2eVME, 2eSST, and 2eSST Broadcast to access multiple VME slaves
- System Controller PRI, RRS, BTO, 2eBTO
- Customization upon request
- Drivers for Windows XP/7, Linux and VxWorks

Overview

IOxOS Technologies is releasing the ALTHEA 7910 solution, a PCI Express x4 GEN1/GEN2 to VME64x transparent bridge embedding a DMA engine that works with on-chip memory and an optional DDR3 external device.

This solution provides a full VME64x Master/Slave interface with Slot-1 functions and interrupt management with a direct bridge to a PCI Express upstream port, assuring an extremely low latency combined with a high data bandwidth. Advanced VME64x data transport 2eVME and 2eSST modes, including broadcast, are natively supported with maximal burst length capability. Large data-transaction buffers guarantee maximal 2eSST data transfer support for continuous operation. A key element for this high performance is an embedded dual channel Intelligent DMA Controller (IDMAC), which allows high bandwidth simultaneous Read/Write transactions exceeding 1'600 MBytes/s data rates with PCI Express GEN2.

The full solution is delivered as an encrypted binary file targeting a Xilinx Artix-7 device (XC7A75T in FGG484 package). The result is a low cost and low power single chip solution which provides higher performance in comparison with existing VME interfaces, a faster integration process and a robust obsolescence management strategy. The implementation, which is done entirely in VHDL, guarantees its portability to coming generations of FPGA devices, significantly extending the operational life of the solution.

The PCI Express to VME64x bridge core function has been successfully implemented and validated in all IOxOS Technologies' VME Single Board Computers since 2009, leveraging Intel x86 (Xeon, i5/i7), AMD (Opteron) and PowerPC (QorIQ P and T series) platforms running under Windows XP/7, Linux and VxWorks. This widespread deployment allows the ALTHEA 7910 solution to reach the high maturity and reliability levels required by the Mil/Aero, Transport and High Energy Physics (HEP) applications where these COTS have been installed.

Due to its long and proven experience in VME design, IOxOS Technologies provides an active support to guide the end user throughout the integration process, considering the customization of the solution upon request.

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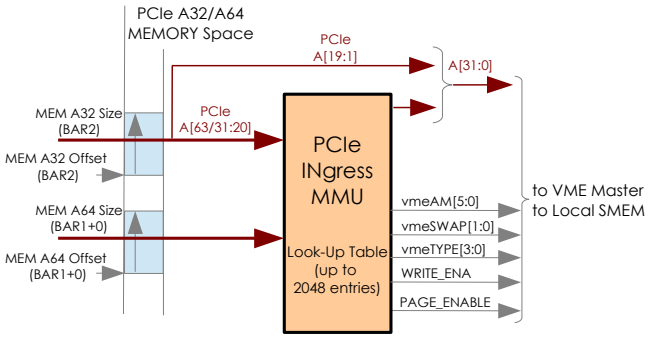
PCI Express Endpoint Interface

The ALTHEA 7910 implements a true PCI Express Endpoint fully compliant with revision 2.1, supporting PCI Express x4, x2 and x1 transfers in both GEN1 and GEN2.

This approach makes possible to have the whole VME address translation space allocated on the PCI Express device tree. This allocation is made through the Base Address Registers (BAR) 4 down to 0 as follows:

- 4 KBytes/256 Bytes IO/Memory Space (BAR4/BAR3) providing access to the Control and Status (CSR) registers
- A32 Non-Prefetchable Memory Space (BAR2) with window size statically programmable from 4 to 128 MBytes
- A64 Prefetchable Memory Space (BAR1+0) with window size statically programmable from 64 to 4'096 MBytes

The relative window size is statically predefined via pin-strapping options and/or EPROM User Configuration area.



The IO space defined by BAR3 and BAR4 is used to map specific CSR registers, whereas the two Memory spaces defined by BAR1+0 and BAR2 provide direct mapping either to the VME64x address space or to the local Shared Memory (SMEM). A MMU like scatter-gather with local translation table is integrated directly in the PCI Express Slave Interface.

The MMU based scatter-gather allows to select per page all VME64x data transactions (SBT, BLT, MBLT, 2eVME and 2eSST) on all common addressing space modes (A16, A24, and A32).

PCI Express Interrupt Support

The ALTHEA 7910 issues PCI Express MSI or Legacy interrupts by means of its embedded Interrupt Controller which can manage up to 64 internal Interrupt sources, including:

- VME IRQ[7:1], SYSFAIL, and ACFAIL
- Location Monitor
- Mailboxes
- Message passing FIFO
- Intelligent DMA Engine (IDMA)
- Local VME64x Errors
- GPIOs

VME64x Master/Slave Controller

The VME interface is handled by a complete VME64x Master/Slave controller with embedded Slot-1 function and a fully programmable byte swapper function integrated in its data path, in order to support efficient little-big endian conversion by hardware.

The operation of the VME Master and Slave controllers is totally independent, providing self-addressing capability and guaranteeing a dead-lock free architecture.

VME64x System Controller

The VME interface is enhanced with a complete VME System Controller (VME Slot-1) featuring the following programmable resources:

- Four(4) level Central Arbiter PRI / RRS
- Timer-based VTON/VTOFF VME access option
- IACK daisy-chain driver
- Programmable BTO/2eBTO
- SYSCLK & SYSRESET* generator

The System Controller can be enabled through static option and/or with VME64x geographic addressing while operating in 64x mode.

The VME AUTO ID mode, allowing to use the 64x CR/CSR with a 3-slot back-plane environment, is also supported.

VME64x Master Controller

The VME64x Master Controller provides optimized access to the VME64x back-plane from following initiators:

- Decoded A32/A64 PCI Express Memory transactions autonomously translated into VME64x Bus transactions
- Register based special RMW transactions
- Embedded IDMA driven transactions

Different modes of operation (write-posting, read-ahead, and read prefetching) can be enabled to fit optimal operation both in terms of latency and of bandwidth performance.

The VME RETRY* Slave signaling is handled for smooth bus dead-lock issue resolution.

The VME Master Controller is linked to a fully programmable VME Arbitration requester module, with BREQ[3:0] level, RWD, ROR and FAIR operation capabilities.

VME Special transactions

The following special transactions are supported through dedicated internal registers:

- ADO, ADOH Address only cycles
- Read Modify Write (Compare and Swap modes)
- VME64x LOCK/ADOH

VME Interrupts

The ALTHEA 7910 embeds a VME Interrupt Handler (INTH) operating either in RORA or ROACK modes.

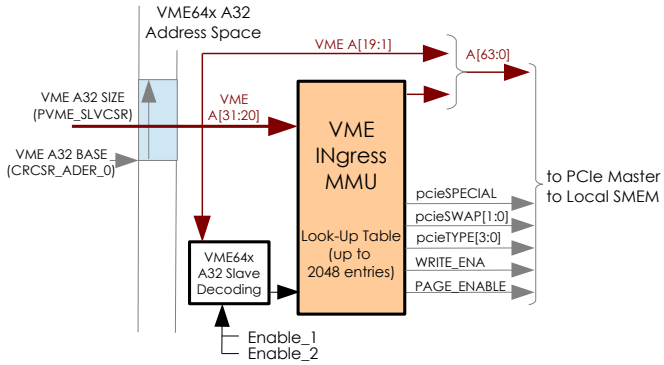
While operating in ROACK mode, a hardware based IACK cycle generator reads the Status_ID from the VME interrupter before signaling the interrupt to the PCI Express host.

VME64x Slave Controller

The ALTHEA 7910 solution provides programmable VME Slave support on two address spaces:

- CR/CSR as defined by the VME64x specification. This 512 KBytes window provides a remote configuration port
- A32 as a programmable window from 1 to 2048 MBytes

A VME INgress MMU access through this window maps the Local Shared Memory and/or the remote PCI Express System Memory.



The controller supports the complete set of VME data transaction types (SLT, BLT, MBLT, 2eVME and 2eSST). It also implements a hardware-based byte swapping capability.

The 2eSST Broadcast mode is also supported, including self-addressing capability.

VME Interrupt Generator

The ALTHEA 7910 embeds a 7-level programmable VME Interrupt generator.

Interrupt Synchronization Resources

Four(4) sets of legacy Location Monitors with interrupt generation capability, mailboxes and message passing FIFOs are also implemented and can be mapped anywhere in the VME A32, A24, and A16 address space.

VME64x Debug Support

Dedicated error tracing registers record the parameters of failed VME transactions for easy error recovery and enhanced embedded debugging support.

VME64x Electrical Interface

The ALTHEA 7910 requires the use of external LVTTL transceivers fulfilling the voltage/current levels required by the VME64x specification.

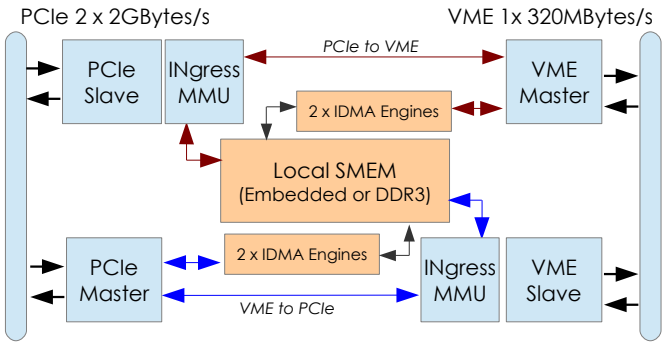
Two different VME electrical interface types, selectable via pin-strapping options, are supported for optimal flexibility and cost/performance ratio:

- LVTH125 + LVTH245 transceivers/buffers
- LVTH125 + VMEH22501A transceivers/buffers

Note VME320 operation over 21-slot back-plane requires VMEH22501A transceivers/buffers

Local Shared Memory (SMEM)

A local memory area is shared between the PCI Express Memory Space, the VME64x A32 Space and the IDMA engines. Thanks to the support of programmable IO MMU, complete address remapping from VME64x and PCI Express, as well as specific protections are supported.



Transactions between the VME Slave and the Local Shared Memory provide optimal performance, latency and deterministic access.

Direct mapping access of the PCI Express attached System Memory from the VME Slave port can exhibit high latency and poor performance, directly related to the chip-set implementation.

The local SMEM is implemented in two ways:

- Embedded SRAM: 128 KBytes of on-chip embedded memory are allocated to build a DPRAM supporting simultaneous read and write transactions for optimal performance
- External DDR3 memory (optional): An integrated multi-port memory controller can access up to 4 Gbit DDR3 x16 device, providing up to 512 MBytes of local SMEM. This optional implementation may be used for applications requiring to move very large amounts of data

Embedded DMA Controllers

The ALTHEA 7910 integrates a dual channel Intelligent Chained DMA engine (IDMA). The DMA engines are tightly coupled with the local SMEM controller, which allows data rates exceeding 1'600 MBytes/s when working with PCI Express GEN2.

The DMA Engines can be programmed to support efficient data move (read-write) between the VME64x, the Local SMEM and the PCI Express Initiator port targeting the Root Complex (RC) System Memory or other attached resources (peer to peer mode).

It is also possible to run direct DMA transfers between PCI Express and VME64x with no intermediate copy in the local SMEM.

Each DMA channel has chaining capability (up to 16 MBytes per chain-descriptor) and is associated to an "End of Transfer" interrupt, coupled with status and time-stamp information. The DMA engines are controlled by a set of registers mapped into the IO space.

The DMA engines implement inter-engine triggering capability. This feature allows to start a second DMA engine on a condition triggered by an operating DMA engine.

Target Device: Xilinx Artix-7 XC7A75T

The ALTHEA 7910 solution is implemented in a Xilinx Artix-7 XC7A75T device featuring a FGG484 package (23x23 [mm]) that is available in commercial, extended and industrial temperature grades (military temperature grade requires the XQ7A100T device).

The delivered programming binary file must be loaded in a 128 Mb SPI Flash EPROM to program the FPGA at power-up. The load can also be done through the PCI Express IO space, allowing to make firmware upgrades of the configured device.

The ALTHEA 7910 uses 1 MByte of this SPI Flash EPROM as user configuration area for device customization purposes, including:

- Static options overwrite (128 Bytes)
- Custom VME64x Configuration ROM (CR) area such as manufacturer ID, board name and revision among others (256 KBytes)
- Cold Reset CSR registers to default values

Additional features can be implemented by IOxOS Technologies upon request in order to support user-specific requirements.

IOxOS Technologies is member of the Xilinx Alliance Program.

Note PCI Express GEN2 support requires a -2 speed grade FPGA

Static Options

The following static options are evaluated at power-up to configure the ALTHEA 7910 operational mode:

- PCI Express Memory and IO window size
- VME System Controller (Enable/Disable)
- VME64x CRCSR mode
- VME Tx/Rx SYSRESET behavior
- VME64x electrical interface type

These static options can be set up via pin-strapping or they can be directly defined in the SPI Flash EPROM user configuration area.

True Time Distribution

A built-in 48-bit timer operating up to 100 MHz can be synchronized with dedicated VME signals, allowing to maintain a true time synchronization among the 21 VME slots using its internal reference or an external one, such as IRIG or GPS.

Additional Services

The ALTHEA 7910 embeds a system monitor with ADC capability to check, among other parameters, VME voltages (±12V, +5V and 3.3V), together with the device temperature. External temperature sensors can also be monitored through dedicated I2C interfaces.

Intel Low Pin Count (LPC) bus, two(2) serial IO (SIO) interfaces and eight(8) GPIO lines are also supported for enhanced connectivity.

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ALTHEA 7910 Device Driver

The ALTHEA 7910 includes device drivers for Windows XP/7, Linux and VxWorks, providing:

- Full access to the device internal registers
- Dynamic management of the 2x512 translation windows allowing transparent access to the VME bus
- Direct control of the DMA engines performing data transfer between PCI Express and VME
- Management of the 64 interrupt sources

The software package also includes a user library implementing the device API, in order to interface the user application with the device driver.

XprsMon Integration Tool

XprsMon is a command interpreter tool for integration purposes. This tool runs in user space and allows the user to:

- Configure the ALTHEA 7910 device
- Exercise all functionality of the interface
- Monitor the VME bus
- Debug the VME setup

Integration Services & DO-254 Compliance

IOxOS Technologies offers proactive engineering services for the ALTHEA 7910 FPGA integration, board level design and software support (OS device driver, libraries and application porting).

An Artix-7 based VME64x board (PEV_7911) featuring a PCI Express External Cabling connection is available to evaluate the ALTHEA 7910 solution as well as to anticipate the development of related software.

For safety critical airborne applications, a DO-254 DAL C compliant certification package can be provided upon request together with support for hardware reviews (SOI) and audits.

Run Time (RT) Licensing Model

The ALTHEA 7910 solution is delivered as an encrypted binary programming file with a predefined number of RT licenses, along with technical documentation (user manual, application notes, and a fully functional reference design), the software kit (device drivers, user libraries and XprsMon integration tool) and one-year technical online support and maintenance.

Ordering Information

Article Reference	*Product Description*
ALTHEA_7910-RT1-C/I/M	100 ALTHEA RT licenses (MOQ) in Commercial, Industrial or Military temperature grade
ALTHEA_7910-RT2-C/I/M	250 ALTHEA RT Licenses
ALTHEA_7910-RT5-C/I/M	500 ALTHEA RT Licenses
ALTHEA_7910-RT10-C/I/M	1K ALTHEA RT Licenses
ALTHEA_7910-RTXX-C/I/M	For higher volume of RT Licenses, please contact IOxOS Technologies