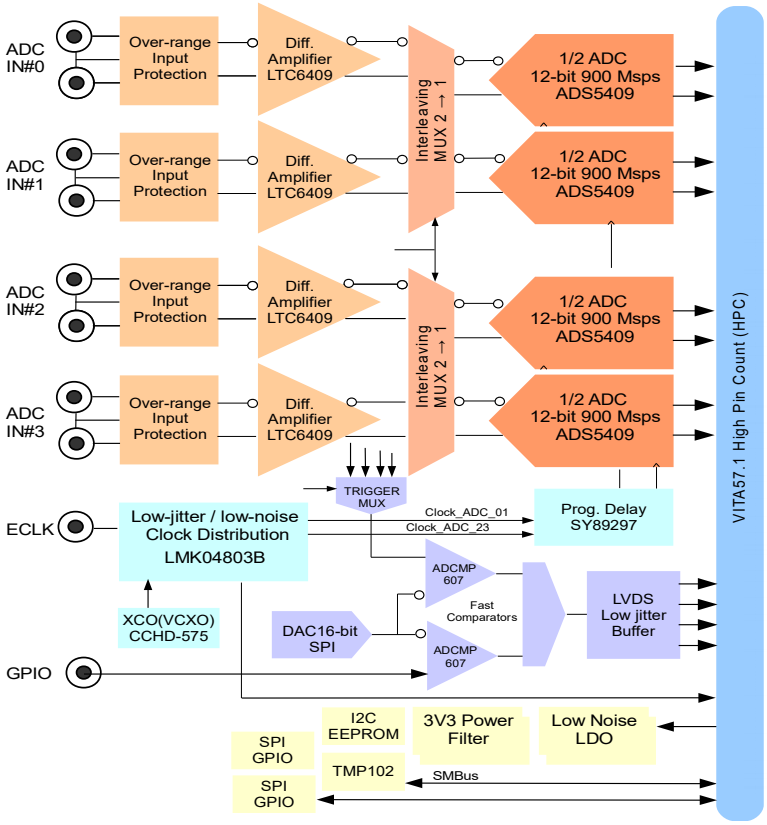
ADC_3112 – Four Channel 900 Msps 12-bit ADC

FMC Mezzanine Board

Data Sheet ADC_3112_DS_A3



Key Features

- Four (4) channels 12-bit/900(1000 with oversampling) Msps ADC
- Differential 100 Ohm DC inputs with >1GHz preamplifier
- Single width FMC VITA 57.1-2008
  - HPC 400 pins connector
  - Ten (10) SSMC front panel connectors
  - 12[W] typical power consumption
- Based on TI latest generation of ADCs
  - ADS5409 dual 12-bit/900 Msps
  - Operates up to 1000Msps with minimal derating
  - Aperture jitter < 100[fs] rms
  - Input bandwidth (-3dB) > 1.2 GHz
- High-end programmable clock tree distribution
  - TI LMK04803 (dual PLL)
  - On-board ultra-low noise oscillator (VCXO/XCO)
  - External SSMC clock reference
- Programmable ADC Clock delay with <100[fs] resolution
- Programmable analog trigger function
  - 250[ps] time tagging precision allowing equivalent time sampling up to 4 Gsps
- XILINX Virtex 6/7 FPGA VHDL Design Kit
- LINUX Software Library

Overview

IOxOS Technologies releases the ADC_3112, a VITA 57.1-2008 form factor module featuring four (4) channels 12-bit 900 (1000 with oversampling) Msps ADC capabilities. This high-density, low-power Gsps class ADC FMC is built on TI latest generation of ADCs, the ADS5409, than can be over-sampled up to 1000Msps with minimal derated performance.

The ADC_3112 is the fourth member of IOxOS Technologies' FMC VITA 57.1 data acquisition product line integrated by the ADC_3110 (16-bit 250Msps ADC with AC coupling), the ADC_3111 (16-bit 250Msps ADC with DC coupling), and the DAC_3113 (high-speed 16-bit DAC).

The four (4) analog inputs are implemented through two (2) SSMC high-frequency connectors configurable as DC coupled differential or single-ended. The high-speed (>1GHz) preamplifier stage, based on LT6409 device, supplies analog signals to the ADS5409 devices and to the analog trigger function.

The on-board clock tree is implemented with a high-precision low-jitter low-phase noise clock fully programmable controller LMK04803B. The clock reference source is selectable either from the front panel SSMC CLKREF input, from the on-board ultra-low phase noise XCO/VCXO or from the VITA57.1 "CLK0_C2M" LVDS signal.

A user programmable GPIO SSMB can also be defined as External TRIGGER, GATE, CLOCK replication or any other user programmable function.

The ADC_3112 targets the following applications:

- Test measurement equipment
- Scientific / Physics experiments

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Introduction

The ADC_3112 is a FMC VITA57.1 module featuring low-power high-density 12-bit/900(1000 with oversampling) Msps ADC capability based on TI latest generation of ADCs, the ADS5409.

Differential DC coupling front-end

The ADC_3112 implements a differential DC coupled input stage, built with low-noise, high bandwidth fully-differential amplifier LTC6409. Single-ended inputs can also be supported through software control. Input differential full scale range is 1.0 Vpp nominal (1.25 max), with 100 Ω impedance.

Each input signal is buffered in differential mode to the interleaving ADC front-end and also to the Trigger programmable comparator.

The interleaving multiplexer function provides a copy of the buffered analog input #1 and #2 to the two ADS5409 devices.

Clock Distribution

The on-board clock distribution is implemented with a low-noise low-jitter dual PLL clock driver, the TI LMK04803B, with clock jitter < 100[fs]. The LMK04803B clock source can be selected from:

- Front panel AC coupled SSMC "CLKREF"
- On-board ultra-low phase noise 100MHz oscillator (Crystek CCHD-575)
- FMC VITA57.1 Carrier "CLK0_C2M"

Seven (7) output clocks, with programmable delay in steps down to 25[ps], are supplied to both ADS5409 devices, to the Programmable Clock Delay SY89297 and to the Trigger Time Stamping logic.

The LMK04803B is fully configurable from the VITA57.1 carrier board.

Programmable Clock Delay

Both ADC ADS5409 clock inputs can be driven through a Programmable Clock Delay SY89297, allowing to adjust the ADC sampling time in steps of 5ps, related to a clock reference.

While operating in interleaving mode, a high-precision low jitter sub-picosecond clock delay logic is provided to the second ADS5409 device, allowing to fine-tuning the 180° anti-phase clock.

Time Trigger Logic

The ADC_3112 integrates an analog trigger function. The four (4) analog inputs and the GPIO SSMC can be routed to a programmable level (DAC8563 value) comparator implemented with an ADCMP607 device. The detected trigger event, selectable as positive or negative edge, is sent to the carrier's FPGA together with a local copy of the ADS5409 clock reference.

Thanks to a dedicated IP core implemented within the carrier's FPGA, the trigger event can be time stamped with a resolution up to 250[ps] (4 times the ADC sampling clock).

For calibration purposes, a reference source derived from the LMK04803B device, with a 25[ps] delay adjustment, can be injected instead of the trigger source.

Power Supplies

The ADC_3112 on-board power supplies are locally built with low noise DC-DC and LDO devices.

A bulk DC-DC generates a local 4.3[V] from the FMC VITA57.1 P3V3 power supply. This local 4.3[V] is used as source for three low-noise LDOs, providing the following voltages:

- Low noise 3.3[V] for ADS5409 devices
- Low noise 1.8[V] for ADS5409 devices
- Low noise 3.3[V] for LMK04803B and VCXO/XCO

The on-board negative power supplies are also generated from a DC-DC to properly feed the low-noise LDOs.

DC-DC operating frequency can be synchronized by the carrier board. One low noise LDO is directly powered by FMC VADJ and generates a local 1.8[V] dedicated to ADS5409 digital read-out section (LVDS).

Other Resources

The ADC_3112 embeds a 256K EEPROM and a temperature sensor TMP102, both connected to the VITA57.1 native SMBus.

TOSCA FPGA Design Kit

IOxOS Technologies has developed TOSCA, a complete FPGA Design Kit optimized for XILINX FPGA devices using VHDL as description language, to interface the ADC_3112 with the carrier's FPGA. In addition, the design environment includes the following functions:

- General DAQ Management
- ADS5409 Data Acquisition up to 1Gsps
- SPI Bus controller for ADS5409, DAC8563 and XRA1404
- uWIRE Bus controller for LMK04803B and SY89297
- Interleaving calibration support
- Trigger Time Tagging at 250[ps] resolution
- GPIO, LED, and basic control functions

Firmware/Software Support

IOxOS Technologies provides a comprehensive product line of VME64x and MTCA.4 FMC carriers, the TOSCA FPGA design environment including FPGA firmware (VHDL sources and binary files), LINUX libraries and data acquisition design examples.

This comprehensive tool allows the implementation of high-performance systems featuring the ADC_3112 modules, through a fully functional application example.

An EPICS driver for this development platform is also available. EPICS drivers are developed by the Paul Scherrer Institute (PSI), and are released upon request under an open source license (http://epics.web.psi.ch/).

IOxOS Technologies also provides design services for the development of custom applications for XILINX based systems.

Consult IOxOS Technologies for more detailed technical data (ENOB, SNR, SFDR Performance).

Ordering Information

Article Reference	*Product Description*
ADC_3112-A0	Dual ADS5409 with on-board XCO 250 MHz
ADC_3112-A1	Dual ADS5409 with on-board VCXO 100 MHz
FDK_3112	FPGA VHDL Reference Design Kit

For other configurations please contact IOxOS Technologies

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RELIABILITY BY DESIGN

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