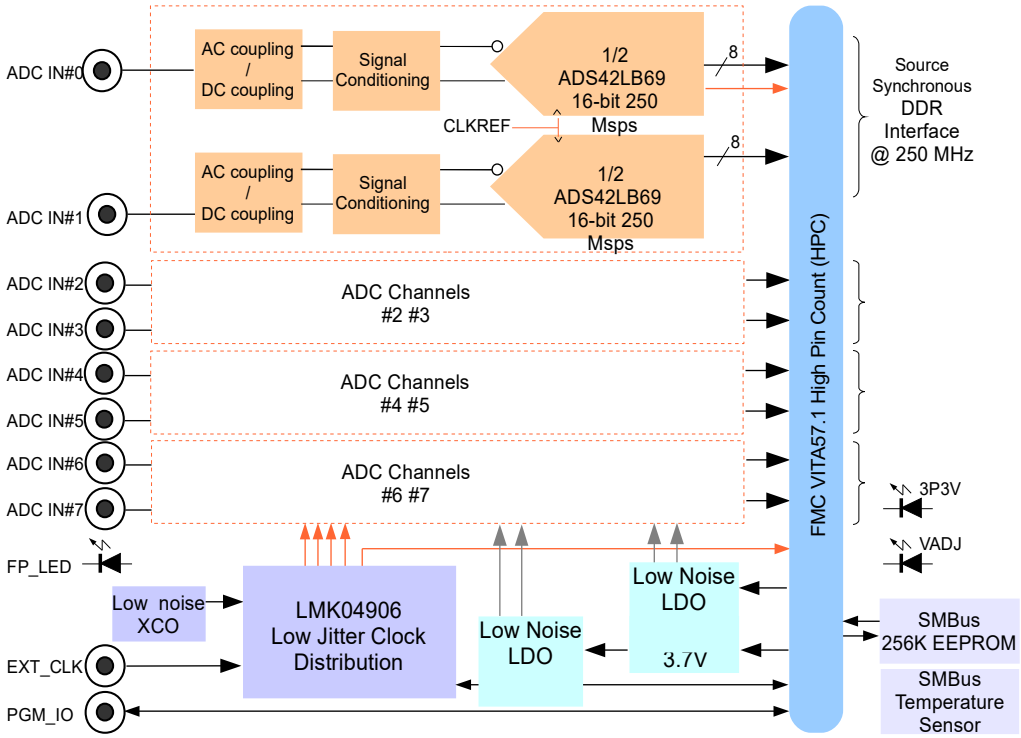
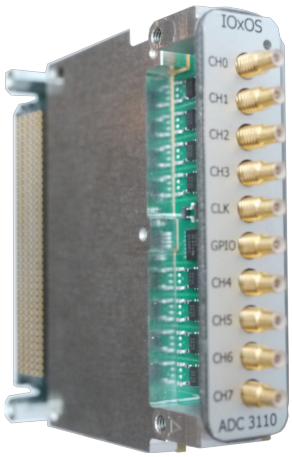
ADC_3110/3111 – Eight Channel 16-bit ADC Data Sheet

FMC Mezzanine Board ADC_3110_DS_A1





Key Features

- Eight (8) channels 16-bit/250Msps ADC
- Single width FMC VITA 57.1-2008
  - HPC 400 pins connector
  - Ten(10) SSMC front panel connectors
  - 8[W] typical power consumption
  - FMC 12[V] power supply not required
  - LVDS high speed interface
- Based on latest generation ADC technology
  - TI ADS42LB69 dual 16-bit/250 Msps
  - Single ended AC coupling (ADC_3110)
  - Single ended DC coupling (ADC_3111)
  - High-speed LVDS data read-out
- Sophisticated clock tree distribution
  - TI LMK4906 (dual PLL)
  - On-board ultra-low noise oscillator /VCXO
  - External SSMC Clock reference
- On board low noise power supplies generation
  - FMC 12P0V power supply not used
- Temperature sensor monitoring through SMBus
- XILINX Virtex 6/7 FPGA VHDL Design Kit
- LINUX Software Library
- Direct EPICS support on IFC_1210 carrier

Overview

IOxOS Technologies introduces the ADC_3110/3111, a VITA 57.1-2008 standard eight (8) channels 16-bit 250 Msps ADC.

The ADC_3110/3111 are the first members of IOxOS Technologies' FMC VITA 57.1 data acquisition product line which includes high speed DAC, GSPS ADC 10/12 bits and programmable digital IO.

The eight(8) single-ended 50 Ohms analog inputs are supplied through SSMC high frequency connectors. AC coupling (ADC_3110) and DC coupling (ADC_3111) versions are available.

Three (3) AC coupling input conditioner schema is also available for optimal target application.

Clock tree is implemented with a high precision on-board low jitter low phase noise clock controller LMK04906 fully programmable by the carrier-board. The clock reference source is selectable from front panel SSMC input or from an on-board ultra-low phase noise XCO/VCXO.

A user programmable LVTTL GPIO SSMB can be defined as TRIGGER, GATE, CLOCK replication or any user defined function.

The ADC_3110/3111 targets the following applications:

- Test measurement equipments
- Radar/Sonar
- Scientific / Physics experiments

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Introduction

IOxOS Technologies introduces the ADC_3110/3111, a FMC VITA57.1 module featuring a high density ADC 16-bit/250Msps based on latest generation TI ADC ADS42LB69.

AC coupling front-end (ADC_3110)

The ADC_3110 50 Ohms AC coupling input schema can be optionally selected for optimal fit to the targeted application.

- Dual BALUN Mini-Circuits TC1-1-13MX+ (default)
- Single RF Transformer Mini-Circuits TC1-1X+

The input range can be selected from 1.5 to 2.5 Vpp by programming the ADS42LB69 reference register.

DC coupling front-end (ADC_3111)

The ADC_3111 implements a 50 Ohms single-ended DC coupling input stage built with ultrahigh dynamic range differential amplifier LTC6409.

The amplifier gain is set to 2.0 and the nominal input ragne is -0.5[V] to +0.5[V].

Clock Distribution

The on-board clock distribution is implemented with a low-noise low-jitter dual PLL clock driver TI LMK04906. The input clock source can be selected from :

- Front panel 50 Ohms AC coupled SSMC "CLKREF" in direct clock input mode
- On-board ultra-low phase noise 100 MHz oscillator (Crystek CCHD-575) in internal clock mode
- Front panel AC coupled SSMC "CLKREF" in PLL refeence mode with on-board VCXO

Five(5) output clocks, with programmable delay in steps of 25ps, are supplied to the four(4) ADS42LB69 devices and to the FMC CLK0_M2C.

The LMK04906 incorporates a uWIRE Bus and is fully programmable from the carrier board FPGA.

Power Supplies

The ADC_3110/3111 on-board power supplies are built locally with low noise devices.

A bulk DCDC generates a local 3.8[V] from the FMC P3V3 power supply. (FMC P12V0 is not used). This local 3.8[V] is used as source for three LDO generating :

- Low noise 3.3[V] for ADS42LB69 devices
- Low noise 1.8[V] for ADS42LB69 devices
- Low noise 3.3[V] for LMK04906 + CCHD-575/VCXO

The DCDC operating frequency can be synchronized by the carrier board.

One low noise LDO is directly powered by FMC VADJ and generates a local 1.8[V] dedicated to ADS42LB69 digital read-out section (LVDS).

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Other Resources

The ADC_3110 also includes two SMBus connected devices:

- EEPROM 256K
- Temperature sensor TMP102 centered on the ADS42LB69 PCB layout

TOSCA II FPGA Design Kit

IOxOS Technologies has developed TOSCA II, a complete FPGA Design Kit optimized for XILINX Virtex 6/7 FPGA devices using VHDL as description language, to interface the ADC_3110/3111 with the carrier's FPGA. In addition, the design environment includes the following functions:

- General DAQ Management
- ADS42LB69 Data Acquisition in embedded DPRAM
- SPI Bus controller for ADS42LB69
- uWIRE Bus controller for LMK04906
- GPIO, LED, and basic control functions

Firmware/Software Support

IOxOS Technologies proposes a development platform made of a high-end VME64x Virtex-6T based FMC carrier, the IFC_1210, TOSCA II design environment including FPGA firmware (VHDL sources and binary files), LINUX libraries and data acquisition design examples.

This comprehensive tool allows the implementation of IFC_1210 based systems featuring the ADC_3110/3111 modules, through a fully functional application example.

An EPICS driver for this development platform is also available. EPICS drivers for IFC_1210 were developed by the Paul Scherrer Institute (PSI), and are released upon request under an open source license (http://epics.web.psi.ch/).

IOxOS Technologies also provides design services for the development of custom applications for XILINX and ALTERA based systems.

Consult IOxOS Technologies for detailed technical data (ENOB, SNR, SFDR Performance).

Ordering Information

Article Reference	*Product Description*
ADC_3110-A0	AC coupling version (dual TC1-1-13MX+)
ADC_3110-A1	AC coupling version (single TC1-1X+)
ADC_3110-A2	AC coupling version (dual TC1-1-13MX+) with on-board VCXO
ADC_3111-A0	DC coupling version
FDK_3110	FPGA VHDL Reference Design Kit

For other configurations please contact IOxOS Technologies